Research Laboratories

Report Number 6890

A Handbook for the 8.448 Mbit/s Digital Multiplex

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ABSTRACT

This report gives the circuit and operational description of an 8.448 Mbit/s plesiochronous digital multiplex designed and constructed in the A.P.O. Research Laboratories.

YN.18/13
Case 12012
Distribution: B, D, L, M.
September 1974

Index Headings:
1. Multiplexing
2. Digital Systems
3. Handbooks

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(R. Smith)
for Director, Research

RESEARCH LABORATORIES - REPORT 6890

HANDBOOK FOR 8.448 Mbit/s DIGITAL MULTIPLEX

1. INTRODUCTION

An 8.448 Mbit/s digital multiplex using +/0/- justification has been designed and constructed in the Line and Data Systems Section of the A.P.O. Research Laboratories.

This report is intended mainly for use as a handbook for the multiplex, but can also be used as a reference for circuit techniques in plesiochronous multiplexers. General principles and theoretical aspects are described in References 1, 2 and 3.

The 8.448 Mbit/s multiplex combines four plesiochronous 2.048 Mbit/s digital input signals. The input signals can come from P.C.M. systems or from multiplexed data signals. The multiplex can be easily modified to accept other input bit rates of up to 2.048 Mbit/s. However, the ratio between input rate and multiplex rate always has to remain $\frac{33}{8}$. Thus if the input rate is changed the multiplex rate has to be changed accordingly.

It is assumed that the reader is familiar with T.T.L. integrated circuits as these form the bulk of the elements used in this particular design. Generally, the descriptions and waveforms do not incorporate propagation times of circuit elements to simplify circuit description. It appeared just possible to design a multiplex with a highest clock frequency of 8.448 Mbit/s with normal T.T.L. integrated circuits. The design included due allowances for maximum and minimum propagation times of all circuit elements. Only the special jitter smoothing circuitry which contains parts that operate at a frequency of 24.576 MHz requires Schottky (S) or High Speed (H) T.T.L. devices. In the multiplex circuitry use is made of an occassional S or H device at critical points for extra margin or for convenience in avoiding the use of extra components.

The circuit diagrams in the back of this report are photographic reductions of standard size drawings. Full size drawings are available on request from the authors.

2. BASIC PRINCIPLES OF +/0/- JUSTIFICATION SYSTEM

In a digital communications network for coded analogue and data signals one of the most important problems is network synchronisation. In order to combine a number of lower bit rate signals into a single higher bit rate stream it is normally necessary that all signals to be combined are synchronous with a single clock source. This method is often impractical, and an easier solution is to have a plesiochronous network. This means that all clocks are autonomous but have frequencies which are within a certain tolerance of a defined nominal frequency. Using this method the bit rate of every tributary of a multiplex node in the network can be equalised by so called justification techniques.

In a +/0/- justification system an input data stream is written into an elastic store and read out using a clock which has nominally the same frequency as the writing clock. Every time there is a one bit phase difference between read and write clocks justification occurs and an

adjustment is made to the read clock to keep it actually the same average frequency as the write clock. When justification occurs, depending on whether the write clock is faster or slower than the nominal rate of the reading clock, an information pulse is inserted (negative justification), or a double reading is made (positive justification). Codes are sent on allotted spaces in the multiplex frame to indicate to the receiver whether there has been positive, negative, or no justification. A space is also allotted for the inserted pulse to be transmitted on the multiplex stream.

3. BLOCK DIAGRAMS

3.1 Transmitter. The block diagram of the Transmitter is shown in figure 1. The Transmitter consists of four cards; 2 identical phase detector & elastic store cards, one common card and one transmit card. The phase detectors and elastic stores for channels 1 and 3 are on one card, and for channels 2 and 4 on the other card.

3.2 Receiver. The block diagram of the Receiver is shown in figure 2. The Receiver consists of eleven cards; an Input card, Common card, Gating card, 4 identical Smoother cards, and 4 identical Buffer - Smoother cards.

4. DESCRIPTION OF FRAME AND MULTIFRAME MAKEUP

In the following description reference is made to figure 14 of the attached drawings.

The multiframe consists of 6 frames, each frame being divided into 2 groups, group 1 and group 2. Group 1 is made up of 256 bits of bit interleaved data followed by an 8 bit frame alignment code. The frame alignment code is transmitted once per frame. Group 2 is made up of 256 bits of bit interleaved data followed by 8 bits of various code and spare bit information. The third, fifth and seventh bits of the last 8 bits in group 2 are spaces allotted for spare bit information which are at present not used. Access has been provided on the multiplex to the spare bits. The multiframe alignment code consists of a 6 bit code spread over six frames in the first bit of the last block of 8 bits in each group 2. Similarly, the justification codes for the 4 channels are sent on bits 2, 4, 6, 8 respectively.

5. TRANSMITTER

5.1 Common Card. In the following description, reference is made to cct 1 of the attached drawings.

The Common card fulfills the following functions. It accepts an 8.448 MHz clock from the Transmit card and produces timing generation, justification code generation, frame and multiframe code generation, and multiplexing of the channel data and associated framing and justification codes.

C1 through to C4 are connected to form a synchronous binary counter clocked by the 8.448 MHz clock. D1(8) detects the state 264, and the generated pulse (A), which is high for 8 bits, is used to clear the first 3 stages. Pulse A is also used as the enable for C4, which first divides A by two (B) and then counts to binary six (C, D, E) at B rate. State 6 is detected by D1(6), and C4 is cleared. D5(4) is used to prevent the enable input to C4 being active during the first half of the clock period, as it was found

that without this precaution faulty operation occurred in this particular configuration. Pulse A occurs at half frame rate, pulse B at frame rate, and pulses C, D and E at multiframe rate. Waveforms are shown in figure 3.

Various pulses need to be generated and sent to the phase detector and buffer cards, and these are produced in the following manner. Refer to figure 4: A clock signal at ¼ the multiplex frequency is generated for reading data out of the buffer. This clock requires gaps in it occurring at pulse A rate for 2 reasons:

1. To reduce its frequency of $\frac{8.448}{4}$ = 2.112 MHz to an effective 2.048 MHz, which is the nominal input clock frequency.

2. A pulse needs to be inserted into this space for justification adjustments.

This clock pulse is produced by gating pulse A with 2^1 in D5(13). A Joint pulse (J) is inserted into pulse A space of the read clock when negative justification occurs to allow the read clock to nominally track the write clock, and to allow an extra information pulse to be read out of the buffer. The Joint Pulse for adjusting the read clock is generated in the last half of the 6th frame, during pulse A high period, and the inserted pulse has the duration of half a 2^1 clock pulse. The appropriate gating is performed in E5(10), D4(12), C5(8), and D5(1). When positive justification occurs a double reading of data is required and a pulse (omit pulse) needs to be omitted from the read clock. Note that for proper timing there are separate Omit pulses for channels 1 + 2 and channels 3 + 4. The Omit pulse for channels 1 + 2 is produced by gating out the last high period of the 2^3 clock in frame 6 and shifting it 2 clock periods at the 8.448 MHz rate by clocking it with the 2^1 clock. The gating and clocking is done via D2(12), D2(8), C5(8), E1(8), and D3(9). Channels 3 + 4 Omit pulse is produced by selecting pulse A in frame 6 and shifting it 4 clock periods at the 8.448 MHz rate by clocking it with the 2^2 clock. The gating and clocking is done via E5(8), D5(10), and D3(5). A justification decision is made during the last half of frame 1 by allowing a "window" of length 8 bits at the 8.448 MHz rate to open at the output of the phase detector. If a justification decision has been made a latch is set on the phase detector card. The set pulse of 8 bits which forms the window occurs just before the start of pulse A in frame one. Gating is achieved via E1(6), D4(6), D2(8), E1(12), E5(12). The latch is reset during the first half of frame 1 at the 2^3 clock rate. Note that the latch is reset a number of times. This was only done to make the circuit configuration simpler. The reset pulse is produced via E1(6), E5(2) and D2(6).

The common card also generates the various framing and justification codes and multiplexes the channel data to form the complete multiplex frame. A number of multiplex IC's are connected as word generators to produce the various codes. B3 produces the multiframe code (110010) which is generated at multiframe rate, and positioned into its correct slot in the framing gaps by A4. A3(9) multiplexes the positive justification commands and uses these to control B2, which produces the positive justification code (000111) under the control of A3(9),

(i.e., when there is a + justification on a particular channel). B2 sends the code via Or gate C5(12) to A4 which inserts the code into its correct slot in the framing gaps. A2(7) multiplexes the negative justification commands and uses these to control B1, which produces the negative justification code (11000X, X = extra information bit) under the control of A2(7) (i.e. when there is - justification on a particular channel). B1 sends the code via Or gate C5(12) to A4 to be multiplexed into the framing gaps. A2(9) multiplexes the extra information bits and sends them to B1 which inserts them into the last bit of the justification code. The no justification code (001100) is derived direct from pulse D off the counter. C5(2) allows this code to be transmitted continuously unless it is inhibited by a positive or negative justification command. On the drawing of frame and multiframe makeup (figure 14) it can be seen that there are spaces for "spare" bits. Normally these are not used, but access has been provided via A4 to allow them to be used if required.

B5 is addressed by pulse A and pulse B and multiplexes the codes to be inserted in the framing gap together with the 4 data streams read out from the buffer, which have been previously multiplexed by A1(7). The frame alignment code (11101000) is produced by B4 and also applied to B5. The output of B5 is retimed via A5 and sent to the transmit card.

5.2 Elastic Store & Phase Detector. In the following description reference is made to cct 2 of the attached drawings.

The Elastic Store & Phase Detector card contains the circuitry required to detect and store a positive or negative justification command. It provides the necessary buffering between the 2.048 MHz rate at which data is read into the buffer, and the irregular 2.048 MHz rate at which it is read out.

Each card contains circuitry for 2 channels, either channels 1 and 3, or channels 2 and 4. Channels 3 and 4 require an inverted read clock, this being the only difference in circuitry between channels. The heart of the elastic store is B5 in which data can be written into any one of 8 bits, and read out from any one of 8 bits simultaneously. A5 addresses the input port of B5 under control of the write clock. C5 addresses the output port of B5 under control of the read clock. B4 is a full adder operating in the two's complement mode in which the read address value (note that this is inverted) is subtracted from the write address value. A gating arrangement at the output of B4 consisting of A4 (2, 8, 10, 12), d4 (8, 11), C4, B3(3) and A1(6), selects the desired subtractions corresponding to negative or positive justification. Gates B3 (8, 11) allow the justification decision that has been made to pass through at set pulse time and be stored in latches A3. B3(6) adds the Joint pulse to the read clock if there has been negative justification; C3(6) omits a pulse from the read clock if there has been positive justification. Monostables D5(4, generate pulses, under the control of the positive edges of the read and write clock, which are slightly longer than the maximum propagation time from C5 and A5, through to the outputs of B3(11) and A1(6). These pulses are added to the set pulse by D3(3, 6), and effectively only allow the detection "window" to open after the propagation time of the detection circuitry.

The phase detection process is shown in more detail in figure 5. The numbers in the squares represent the relative count states of the read and write counters. Taking the write clock as a reference, the read clock can be said to be so many counts behind the write clock. If the 2 clocks are nominally the same, the normal range of the read clock varies between 4 and 3 counts behind the write clock, which allows for the framing gap. If the write clock is slower in frequency than the read clock, the read clock will slide to the left. Depending on the amount of frequency difference, the read clock could be 2, 1 or 0 counts behind the write clock at the point of justification detection. Conversely, if the write clock is faster in frequency than the read clock, the read clock will slide to the right. Depending on the amount of frequency difference, the read clock could be 5, 6 or 7 counts behind the write clock at the point of justification detection.

5.3 Transmit Card. In the following description reference is made to cct 3 of the attached drawings.

The transmit card generates the 8.448 MHz, crystal controlled, master clock for the system and distributes it to the various cards. It also converts the binary multiplexed data stream from the Common Card into a HDB3 bipolar code, at 75Ω output impedance, which is then suitable for line transmission.

TR 1, with associated components form the 8.448 MHz crystal controlled oscillator. TR2 and TR3 are connected as a differential pair being used to square up, and provide a symmetry adjustment, for the output of the oscillator.

The transmitter incorporates a HDB3 code converter to alleviate the problem of long sequences of zeros in the multiplexed stream, which cause the receiver great difficulty in extracting the clock component. A HDB3 code differs from the normal bipolar code only if the message contains sequences of 4 or more zeros. With the HDB3 code special 4 bit sequences replace sequences of 4 consecutive zeros in order to fill in pulses for the zeros. The following are the HDBn coding rules:-

1. The elements of the inserted sequence are zeros, with the exception of the first and last one.

2. The last element is always a one and its polarity chosen such that it violates the bipolar law.

3. The first element is either a zero or a normal bipolar one. It is chosen such that the number of ones between any consecutive violation pulses is odd. Thus, if the number of "ones" between 2 insertion sequences is even, the insertion sequence is started with a "one"; if the number is odd, the sequence is started with a "zero".

4. The first "one" after the inserted sequence follows the normal bipolar rule.

B3 operates as a 4 stage shift register with B4(8) monitoring the zero contents of the register. Until a sequence of 4 zeros is received the output of B4(8) is held high, thus C4(11) acts as an invertor. The output of C4(6) is held high, C5(2) is held high, and C5(11 and 3) act purely as invertors. C5(6), B5(5, 6),

and C3 are a conventional bipolar output circuit. When a sequence of 4 zeros is received B4(8) output goes low, bringing the HDB3 coding into effect in the following manner. C4(11) is forced high, which after the next clock pulse, converts the last element of the sequence to a one, satisfying part of rule 2. C4(4) is opened allowing the state of B5(9) to be transferred through to C5(11). B5(9), together with C5(8) has been counting the number of ones between successive insertion sequences. This causes the first element to change via C4(6) and C5(11) according to rule 3. C5(3) is included to prevent B5 from toggling before the last element of the sequence arrives satisfying the second part of rule 2. An example of HDB3 coder waveforms is shown in figure 6. A well designed bipolar output stage should have a constant output impedance for the 3 output states. In the particular configuration used here the output impedance is correct for the positive and negative output pulse states, but is high for the zero output state. Allowing for its deficiencies this output stage is used generally because of its simplicity.

6. RECEIVER

6.1 Input Card. In the following description, reference is made to cct 4 of the attached drawings.

The Input card performs the following functions. It extracts the 8.448 MHz clock component from the incoming stream, converts the bipolar stream to unipolar, and decodes the HDB3 code. It also generates a 24.576 MHz clock using a phase-locked loop, for use in the smoothing circuitry.

The bipolar input stream is applied via L3 to TR1 and TR2, whose function is to "pump" coil L1 every time a one is received. L1 is tuned to the clock frequency (8.448 MHz), and has a Q of approximately 100. Comparator A3 is fed from a tapped off portion of L1, and is used to square up the output of L1 to T.T.L. levels. The clock is then fed to various points via B3(6, 8, 10, 12). TR 3 and TR4 convert each half of the bipolar stream into T.T.L. levels, which are combined in B4(6) to form a half width unipolar stream. D4, B3(2, 4), and B4(11, 8, 3) form the bipolar violation checker. D4 is clocked every time there is an incoming one, and is arranged so that its outputs toggle via inhibit gates B4(11, 8) only under the no violation condition. B4(3) output therefore stays low. When a violation occurs, D4 does not toggle on the violation pulse, and one of the gates B4(11 or 8) allows the violation pulse to pass through to B4(3). Typical waveforms are shown in figure 7.

The unipolar data stream is fed into shift register D5. If a violation pulse is present at E5(9), and at the same time D5(6) and D5(11) are high, D5 is cleared via B2(6) to remove the unwanted HDB3 code information. E5(9), together with E1(3, 6, 11), retime the violation pulses, providing pulses which last approximately the high period of the clock pulse. Typical waveforms are shown in figure 8.

The circuitry used for reducing multiplex jitter requires a frequency to be generated at 12 times the nominal tributary frequency, i.e., 12 x 2.048 = 24.576 MHz. It is generated according to the following formula:

$$\frac{8.448}{11} \times 32 = 2.048 \times 12$$

The 8.448 MHz clock is divided by 11 by D3 and applied to a phase-locked loop to multiply this frequency by 32. C4(9), connected as ÷ 2, and A2 connected as ÷ 16, form the ÷ 32 feedback loop in the system. C3 is a latch type digital phase detector and a charge pump, the charge pump being used to convert the T.T.L. levels out of the phase detector into analog levels suitable for controlling the V.C.O. C2 with associated components form the amplifier and low pass filter. D1(2) and associated components form the 24.576 MHz voltage controlled, crystal oscillator. D1 is a varactor diode, which under the control of the output of the amplifier and low pass filter, varies the capacitance in series with the crystal. D1(14) is a buffer for the output of the oscillator. Invertors A1(4, 6, 8, 10) are connected in parallel to increase the driving capability of the 24.576 MHz clock. The phase-locked loop has an ω_n of 95Hz, a damping factor of 0.7 and a total D.C. gain of 2.3×10^4.

6.2 Common Card. In the following description reference is made to cct 5 of the attached drawings.

The Common card provides timing generation, frame and multiframe synchronisation and extracts the spare bit information from the multiplex stream.

A1, B1, C1, D1, are connected to form a synchronous binary counter clocked by the 8.448 MHz clock. B2(8) detects state 264 and the generated pulse (A), which is high for 8 bits, is used to clear the first 3 stages. Pulse A is also used as the enable for D1, which first divides A by two (B), then counts to binary six (C, D, E) at B rate. State 6 is detected by D2(8), which clears D1. Waveforms are identical to those shown in figure 3. D5(5) is connected to the load pulse to prevent the first three stages of the counter from clearing at the instant the counter should be loaded for frame synchronisation. F5(8) prevents state 6 from clearing D1 (at the instant the counter should be loaded for frame synchronisation) and also prevents D2 from generating a clear pulse during the first half of the clock period. It was found that this could cause faulty operation in this particular configuration. C2(8) allows D1 to be cleared by state 6 or by a pulse produced for the multiframe synchronisation.

System synchronisation is controlled by the following factors:

1. Loss of frame synchronisation or multiframe synchronisation is assumed to have taken place when four consecutive synchronisation signals have been received in error.

2. In cases where frame synchronisation is assumed lost, the alignment system will assume synchronisation after first detecting the appearance of 2 successive error free frame alignment signals in their correct positions. When multi-frame synchronisation is assumed lost, the alignment system will assume synchronisation after the detection of one error free multiframe alignment signal.

3. Frame and Multiframe re-synchronisation processes are independent.

The framing synchronisation circuitry operates as follows. Assume that frame synchronisation has been lost. Monostables D3 (4, 12) will both be high, causing D5(8) to be low and D5(11) to be high. This allows an unrestricted movement of data into the B input of shift register B5, B2(2, 4, 6), C4(2) and B4 detect the frame alignment code producing a low going pulse, hereafter called the load pulse, of one clock period duration at the output of B4. As D3(2) is low, the other input (1) is blocked. On the positive going edge of the load pulse monostable D3(12) is triggered and produces a pulse of duration slightly more than one frame length. D3(12) goes low, forcing D5(8) high, which in turn opens D3(1) and opens gate D5(11). D5(11) is now under control of D4(3), which is gated with A and B to select the next frame alignment code position. The load pulse sets the frame counter in synchronisation with the incoming information, and also loads the multiframe counter back on its current state to avoid upsetting the multiframe count. Input A of B5 is opened at the position that the next frame alignment code should occur. If the code does not occur Monostable D3(12) drops back to its original state and the system starts the searching sequence over again. If the code does occur, the load pulse is generated from B4(8) as before.

D3(1) is now open, so on the downgoing edge of the load pulse this monostable is fired. D3(4) goes low clearing D3(12), and taking over control of D5 from D3(12). D3(4) is timed to be slightly more than 4 frame periods to allow for transmission errors in the code. Note that D3(4) is a retriggerable monostable, meaning that each load pulse will retrigger the monostable, holding the output in its triggered state, but recommencing the timing from the last trigger pulse. The load pulse is still applied to the timing counter every frame as a self checking arrangement. If a burst of more than 3 successive frame alignment codes are in error D3(4) drops out and the searching sequence commences afresh. Typical waveforms are shown in figure 9.

The multiframe synchronisation circuitry operates as follows. Assume that multiframe synchronisation has been lost. E1(13) is low causing D4(11) to be high. Gate C2(6) allows C3(12) to be active when pulse B is low and CH_1C is high. Pulse CH_1C is added to effectively terminate the end of B earlier so D1 does not clear in the wrong position. (See figure 10 for position of CH_1C). A clock is generated at multiframe rate and at the position that the multiframe code should occur (see figure 10). Data is shifted into C5. C4(4, 6, 12) and C3 detect the multiframe alignment code if allowed by C2(6). The pulse out of C3 is used to clear counter D1 via C2(8) setting the multiframe counter in synchronism with the incoming information. On the upgoing edge of the pulse out of C3, E1(13) is triggered causing its output to go high. E1(13) is timed to be slightly more than 4 multiframe periods to allow for transmission errors in the code. If the receiver is in multiframe synchronisation, E1(12) will generate a pulse in the first half of frame 1 of approximately 250 ns duration. This pulse can now pass through D4(11) to C3(11) opening C3 during the first half of frame 1 to detect the next multiframe alignment code.

If a burst of 4 or more multiframe codes is in error E1(13) drops out and the searching sequence commences afresh. The output of C3 is applied to D1 every multiframe as a self checking arrangement. C2(11) combines the outputs of the 2 synchronisation detectors and via TR1, turns the "In Sync" lamp off if one or the other is out of synchronisation.

Various pulses and clocks need to be generated and fed to points in the receiver. They are generated in the following manner (ref. to figure 10). Channel clocks at a 2.112 MHz rate with frame gaps need to be provided to take individual data streams from the multiplexed data stream. The channel clocks are generated in B3 which is controlled by pulse A to form the framing gaps. Omit pulses are required for channels 1 and 2 and channels 3 and 4 to control the channel clocks when positive justification occurs to avoid a double reading of data. Omit 3 and 4 is generated by gating out the last pulse A in frame 6 using B2(6), shifting it using the 2^2 clock, and then shifting it again using the 2^1 clock. The Omit 1 and 2 pulse is generated by shifting using the 2^2 clock as for Omit 3 and 4, and gating this pulse with Omit 1 and 2. A reset pulse is required for resetting the command latches, and for use as the timing pulse in the multiframe synchronisation circuitry. This is generated by shifting Omit 3 and 4 using the 2^2 clock, and using the downgoing edge to trigger E1(12) monostable whose duration is approximately 250 ns. When negative justification occurs extra pulses are added to the channel clocks to read out the inserted information. The extra pulses are generated by A3, and occur only when pulse A and pulse B are high, as determined by D4(6). D4(8) selects frame 6 and controls A5, to allow the read pulses through only on frame 6. A clock burst of 4 pulses at frame rate is required to clock out the justification command information. The individual pulses are generated by A3, and combined by D2(6). A3 also generates the clock for shifting in the multiframe alignment code.

To read out the Spare bit information, clocks are required at frame rate, occurring at the Spare bit position. These are provided by A3. E5(7) and A2 are used to clock out the Spare bit information.

6.3 Gating Card. In the following description reference is made to cct 6 of the attached drawings.

The Gating card performs the function of extracting the justification information, for each channel, off the incoming data stream. Majority gating is used to allow for one bit error on any of the justification codes.

B1, C1 and D1 form a 24 bit shift register clocked by a clock burst of 4 pulses occurring at the justification code positions at frame rate. The outputs of the shift register are tapped off at the 1st, and then every 4th output. The negative justification codes are detected by gates D3, E1, and D2, and fed via E5 (12, 8) to B3(9, 10, 11, 12), which demultiplexes the code information of the 4 channels. Gates A1 and A2 are connected as latches to store the command information until they are reset. A5(12) selects frame 5 and also selects the justification code positions. The output of A5(12) is delayed one 8.448 MHz clock period by B5(8) to allow for propagation times and

is then applied to E5(10) to select the code information. E5(11) only allows justification code information to be detected when the system is in synchronisation. B3(9, 10, 11, 12) is inhibited when the 8.448 MHz clock is low, to allow for propagation times. Typical waveforms are shown in figure 11.

The gating for negative justification is derived as follows:

$C_{-} = 1 . 1 . 0 . 0 . 0 . \underline{X}$ X = extra information bit.

$b . c . \bar{d} . \bar{e} . \bar{f}$

(Allowing for 1 bit error) $= b c \bar{d} \bar{e} \bar{f} + \bar{b} c \bar{d} \bar{e} \bar{f} + b c d \bar{e} \bar{f}$
$+ b \bar{c} \bar{d} \bar{e} \bar{f} + b c \bar{d} \bar{e} f + b c \bar{d} \bar{e} f$
$+ (b + \bar{b}) c \bar{d} \bar{e} \bar{f} + (c + \bar{c}) b \bar{d} \bar{e} \bar{f} +$
$(d + \bar{d}) b c \bar{e} \bar{f}$
$+ (e + \bar{e}) b c \bar{d} \bar{f} + (f + \bar{f}) b c \bar{d} \bar{e}$
$= c \bar{d} \bar{e} \bar{f} + b \bar{d} \bar{e} \bar{f} + b c \bar{e} \bar{f} +$
$b c \bar{d} \bar{f} + b c \bar{d} \bar{e}$

The positive justification codes are detected in gates B2, C3, C4, C5, D4, D5, B4, and applied to B3(4, 5, 6, 7) which demultiplexes the code information of the 4 channels. Gates A4 and A3 are connected as latches to store the justification information until they are reset. A5(8) selects frame 6, and also selects the justification code positions. The output of A5(8) is delayed one 8.448 MHz clock period by B5(6) to allow for propagation times, and applied to the input of the majority gating network. The input to the majority gating network is also gated with the "In Sync" condition to allow code information to be detected only when the system is in synchronisation. B3(4, 5, 6, 7) is controlled with the 8.448 MHz clock, letting information into B3 only when the clock is low, to allow for propagation times. Typical waveforms are shown in figure 11.

The gating for positive justification is derived as follows:

$C_{+} = 0 . 0 . 0 . 1. 1. 1.$

$\bar{a} . \bar{b} . \bar{c} . d . e . f$

(Allowing for 1 bit error)

$= \bar{a} \bar{b} \bar{c} d e f + a \bar{b} \bar{c} d e f + \bar{a} b \bar{c} d e f$
$+ \bar{a} \bar{b} c d e f + \bar{a} \bar{b} \bar{c} \bar{d} e f + \bar{a} \bar{b} \bar{c} d \bar{e} f + \bar{a} \bar{b} \bar{c} d e \bar{f}$
$= (a + \bar{a}) \bar{b} \bar{c} d e f + (b + \bar{b}) \bar{a} \bar{c} d e f + (c + \bar{c}) \bar{a} \bar{b} d e f$
$+ (d + \bar{d}) \bar{a} \bar{b} \bar{c} e f + (e + \bar{e}) \bar{a} \bar{b} \bar{c} d f + (f + \bar{f}) \bar{a} \bar{b} \bar{c} d e$
$= \bar{b} \bar{c} d e f + \bar{a} \bar{c} d e f + \bar{a} \bar{b} d e f$
$+ \bar{a} \bar{b} \bar{c} e f + \bar{a} \bar{b} \bar{c} d f + \bar{a} \bar{b} \bar{c} d e$

6.4 Buffer - Smoother Card. In the following description reference is made to cct 7 of the attached drawings.

The function of the Buffer - Smoother card is to generate a read clock for the channel buffer using the positive and negative justification commands. The channel buffer allows data to be read in at an effective 2.048 MHz (actually a 2.112 MHz clock, with gaps at pulse A rate), and read out using a smoothed 2.048 MHz rate. It also contains part of the smoothing circuitry used to generate a 2.048 MHz clock from a divided down 24.576 MHz clock. Note that there are 4 Buffer - Smoother cards, one for each channel.

A clock is required for clocking data off the multiplex stream and into the buffer. This is done with a 2.112 MHz clock with framing gaps in which pulses can be added or deleted under the control of the justification commands. A channel clock is applied to A3(4). If positive justification occurs A3(8) allows an Omit pulse to be applied to A3(5). This deletes one clock pulse from the channel clock. If negative justification occurs A3(11) allows an extra read pulse to be applied to A3(1) and to be added to the channel clock (see figure 10).

The channel clock is then used to clock a counter (B3) which addresses the write input of the buffer, and also to clock the channel data off the multiplex stream (via A1(5)) to be read into the buffer. A2(3) gates together the negative justification command and the Omit pulse. A2(6) adds this and A3(6) together to provide a pulse whenever positive or negative justification occurs. This pulse which has the length of the Omit pulse, is called the Smoother Latch pulse and is used in the smoothing card and also to clock A1(9). A1(9) gives a high when positive justification occurs, and a low when negative justification occurs, and is used to control the add/subtract action in the smoother. D5(12) produces a load pulse, controlled by the Smoother Latch pulse, to be used in the smoother. C3 is clocked by a smoothed clock and addresses the read output of the buffer at a 2.048 MHz rate. Some mechanism needs to be employed to ensure that reading and writing do not occur at the same position, and to correct the reading position back to its nominal position, if the reading location shifts, or is not correct during initial setup. The correction of the reading location is done as follows. C3 addresses D4 to produce 8 outputs, each of one bit duration, corresponding to the 8 counter states. B5(12) detects the 0 state of the write counter. Under the correct read/write conditions of the buffer, the read counter is set to read between states 3 to 5 relative to state 0 of the write counter. A4(6) is then high at the same time that B5(12) is detecting the 0 write state. A4(11) is therefore low resetting latches C4 at intermittent intervals. Both inputs to A5(8) are high, thus inhibiting A5(11) and preventing the buffer from being corrected.

Assume that for some reason the smoothed clock frequency increases, the read clock counter will slide towards state 7 or 0. When it hits state 7 or 0 A4(3) is activated, which in turn changes the state of latch C4(8) via A4(8). A5(8) is therefore forced high opening gate A5(12) and allowing pulse A through, to apply a "subtract" adjustment to the smoothed clock, decreasing its frequency. A2(11) is also forced high which directs the smoothing circuitry to set up the condition for decreasing the smoothed clock frequency. The smoothed clock is continually decreased in frequency until state 5 of the read clock counter is

reached, at which point A4(11) is activated, the output of which resets latch C4(8). This in turn, via A5(8), forces A5(11) high, stopping the frequency adjustment. The read counter therefore has slid back to state 5 and the nominal read/write position is reached. If the smoothed clock frequency decreases the read clock counter will slide towards state 2. A similar adjustment procedure will occur as previously except that the smoothed clock will increase in frequency until the counter reaches state 3 when the adjustment is stopped and the nominal read/write position is reached.

The smoother section on this card works in conjunction with the smoother card to reproduce the input 2.048 MHz ± Δ clock with a minimum amount of multiplex jitter. Briefly, the smoother card (described in more detail later) divides the distance between the justification commands received into 12 equal sections. The smoother section on this card then makes an add/subtract type adjustment, 12 times per command, to a clock generated at 12 times 2.048 MHz. This adjusted higher clock is then divided by 12 to bring it back to the input clock frequency of 2.048 MHz ± Δ.

The output from the smoother card ($C_{+/-}$) is fed into D2(13). D2(12) allows the smoother card output, and if necessary the buffer overflow mechanism, as described earlier, to control the frequency adjustment of the smoothed clock. When there is no frequency adjustment occurring, E1(6) is low, (having previously been preset) D1(5) is low inhibiting D2(6, 8), and forcing its outputs low. C1(6, 8), are high, causing B1(5, 6) to act as a straight divide by 2. B1(9) divides by 2 again, and D3 divides by 3, making a total divide by 12 to obtain a nominal 2.048 MHz clock. When a pulse arrives at E1(1), on the negative going edge a high is clocked through to E1(6). On the next 24.576 MHz clock pulse a high is clocked through D1(5) and opens one of gates D2(6, 8). A2(11) determines which of D2(6, 8) gates will be opened. If A2(11) is high (positive justification), D2(8) will be opened, if it is low (negative justification), D2(6) will be opened. Note that the states of B1(5, 6) also determine which of gates D2 will be opened, but as these states alternate each clock period, each D2 gate will only be allowed to open every second clock period. If D2(8) is opened a high appears at the input to C1(11). After the next clock pulse C1(8) goes low, causing B2(6) to go high, and presetting E1(6) to low via C2(4). After the next clock pulse C1(8, 9) is reset, D1(5) goes low, B1(5) is held low for one extra clock period, thus holding B1(9) low longer, and effectively reducing the divided frequency (nominally 2.048 MHz) by 1/12th of a pulse. The inclusion of D1(5) may appear unnecessary. D1 was added to ensure that positive transitions could not occur at the J inputs to C1 during the set-up time of C1, otherwise faulty operation occurred. If D2(6) is opened a similar situation occurs except that C1(5, 6) are affected, causing B1(5), and thus B1(9), to be held high for one extra clock period. This effectively increases the divided down frequency (nominally 2.048 MHz) by 1/12th of a pulse. Typical waveforms are shown in figure 12. E1(8) and D1(8) are monostables provided to give a minimum defined length to the $C_{+/-}$ pulses. The $C_{+/-}$ pulses trigger E1(13) and D1(8) is used to clear a counter on the smoothing card which produces the $C_{+/-}$ pulses, thereby terminating the $C_{+/-}$ pulses.

6.5 Smoother Card. In the following description reference is made to cct 8 of the attached drawings.

The Smoother card counts the distance between commands and divides this distance into 12 equal parts, generating 12 equally spaced pulses (via the buffer and smoother card). It also makes allowance for a change in the distance between successive commands by storing the number of $C_{+/-}$ pulses which would have been lost because of the change in the distance between commands, and distributes these pulses when space permits.

As the justification command rate can only vary in multiples of a multiframe it is sufficient to count at multiframe rate. A1, B1, C1, D1, are connected as a 16 bit synchronous counter clocked by pulse E, which occurs at multiframe rate. The multiframe counter is cleared, every time a justification occurs, by the Smoother Latch pulse via D5(10). Just before the multiframe counter is cleared, the information on the outputs of the multiframe counter is stored by A2, B2 and C2 on the rising edge of the Smoother Latch pulse. New information is stored every time a justification occurs. Another counter consisting of A4, B4, C4 and D4, counts at pulse A rate which is 12 times pulse E rate. The outputs of the pulse A counter are compared with the outputs of the stored information of the multiframe counter in A3, B3 and C3. If the 2 outputs of the counter are equal a $C_{+/-}$ pulse will be generated just after the downgoing edge of pulse A. The $C_{+/-}$ pulse is sent to the Buffer - Smoother card to initiate the add/subtract adjusting procedure as described earlier. The $C_{+/-}$ pulse is then sent back from the Buffer - Smoother card via a monostable to clear the pulse A counter and terminate itself. Because the pulse A counter is asynchronous, C5(6) is gated with pulse A to ensure that spikes cannot occur at C5(6). D5(12) ensures that the multiframe counter holds its maximum count if the command rate is lower than the capacity of the counter allows to count.

As the distance between successive commands can change, extra circuitry is required to ensure an average of 12 $C_{+/-}$ pulses between commands. To ensure that on average enough $C_{+/-}$ pulses are generated the Smoother Latch pulse is applied to C5(9) thus providing a $C_{+/-}$ pulse when a command occurs. A5 and B5 ensure that on average 12 $C_{+/-}$ pulses are generated between commands by inhibiting C5(6) in case too many $C_{+/-}$ pulses are generated.

If the distance between 2 successive commands increases, on the first increased distance, too many $C_{+/-}$ pulses will be generated but they will be blocked by gate C5(6), controlled by counter A5. Conversely, if the distance decreases, not enough $C_{+/-}$ pulses will be generated. The latter deficiency is corrected for by the use of A5 and B5. A5 is a binary counter used to count the $C_{+/-}$ pulses. B5 controls the storing of the number of $C_{+/-}$ pulses which would have been lost. This is done by reloading the state of A5, to allow A5 to control the number of pulses through C5(6) on the next longer command distance

when an oversupply of $C_{+/-}$ pulses occurs. Three cases are to be considered.

1. When the distance between commands is constant A5 is organised via B5 to commence counting (after the Smoother Latch pulse arrives) at state 4. A5 then counts 11 $C_{+/-}$ pulses, at which point the carry is enabled, inhibiting gate C5(3), thus preventing further pulses being used from the comparison circuitry. The 12th pulse is provided by the inserted Smoother Latch pulse. As the load pulse and the Smoother Latch pulse occur simultaneously, the Smoother Latch pulse clocks A5 whilst the load is enabled, loading A5 into state 4. The adder (B5) feeds state 4 to A5 by adding state 15 of A5 (which is the state at which A5 carry is enabled) to a fixed state 5. As a result of the addition state 4 is then produced.

2. If the distance between 2 successive commands increases, counter A5 will count to 15 and enable the carry, thus preventing passing of further $C_{+/-}$ pulses through C5(6). The counter started at state 4 and counted to state 15. This means 11 $C_{+/-}$ pulses have been counted. On receipt of the next command the Smoother Latch pulse will provide the 12th pulse via C5(8), and together with the load pulse, load A5 into state 4. It can therefore be seen that if the distance between successive commands increases, the correct number of $C_{+/-}$ pulses are produced.

3. If the distance between 2 successive commands decreases, counter A5 will not be able to count to 15 before the next Smoother Latch pulse arrives, causing a deficit in the number of $C_{+/-}$ pulses produced. On receipt of the next command B5 will therefore add a lower number to 5 producing a lower number for counter A5 to commence counting from. When the next longer command distance occurs, the stored number allows extra $C_{+/-}$ pulses to pass through C5(6) to make up the deficit. This particular command distance will thus contain 12 plus the deficit $C_{+/-}$ pulses. Typical waveforms and adder operation are shown in figure 13 and below.

Number of Multiframes between Commands:	3.	3.	4.	3.	4.	4.	3.	3.
State of A5 before loading:	15.	15.	15.	12.	15.	15.	12.	12.
State of B5 before loading:	4.	4.	4.	1.	4.	4.	1.	1.
Number of $C_{+/-}$ pulses produced:	12.	12.	12.	9.	15.	12.	9.	12.

When the justification rate is increased to more than half the available capacity a storing capability of 6 is required. As the adder and counter of the prototype multiplex are designed to store a maximum deficit of 4, under the condition of a justification rate of more than half justification capacity, not enough $C_{+/-}$ pulses are generated and the smoothed clock will slip. The buffer

adjusting mechanism will then come into operation (see Buffer - Smoother card) to prevent data slip. The buffer adjusting mechanism works as a safeguard, as under normal conditions the justification rate will always be less than half maximum rate. However to minimise output jitter for jittered input signals with phase change rates up to the maximum justification rate of 2.6 KHz, a storing capability of 6 is necessary.

Formulae for working out adder size, and other factors are shown in section 7. The principles of the smoothing are more generally described in Ref. 3.

7. MODIFICATIONS FOR JUSTIFICATION COMMAND AVERAGING (SUMMING)

In the following description, reference is made to cct 9 of the attached drawings which shows the modifications to be made if summing is required.

Justification command averaging might be obtained by summing the distances between the justification commands to attempt to reduce the effect of varying distances between commands. Summing is carried out by dividing the received command rate. It is thought (and partly proved by measurements) that summing will reduce the effect of input jitter. Some disadvantages of summing are that the frequency of the multiplex jitter is reduced (making further reduction of jitter even harder), and tracking at very low justification rates takes longer.

To implement summing in the receiver, modifications need to be made to the Smoother card and the Buffer - Smoother card. One output channel has been provided with all necessary modifications. Programming for s = 0,8,12,22 is performed with pre-strapped sockets.

On the Buffer - Smoother card a divider, dividing by the summing rate s, needs to be added between A2(6) and D5(10). The smoother latch output is also divided by the same amount. Dividing is performed by E5 and F5, acting in a load, count-up, carry-load mode. A facility for changing the division factor by 8, 12 and 22 is also shown.

On the smoother card a number of modifications need to be made. Firstly the $\bar{A}$ pulse used in the no summing condition has to be increased in frequency by factors of 8, 12, and 22. In addition these new pulse rates have to be synchronised to the $\bar{A}$ pulse rate. H4 and G4 form a binary counter clocked by the 8.448 MHz clock. Monostable H3(4) produces a narrow pulse triggered by pulse $\bar{A}$ to load the counter into the zero state. The outputs of the counter are compared in H5 and G5 with a number which is set up by the strapping arrangement. When the counter output equals the number set up by the strapping, G5(6) goes high, which then clears the counter, causing G5(6) to go low. This arrangement thus produces the required clock rate in a programmed fashion. H3(12) monostable is triggered every time a comparison is made and is used to generate a pulse the same polarity and duration as pulse $\bar{A}$.

As the pulse rate on pin 22 of the Smoother card is increased, more $C_{+/-}$ pulses are generated between commands. The size of the adder therefore needs to be increased as the summing rate is increased. Adder size, and also the fixed number added to the $C_{+/-}$ counter outputs can be varied by changing the strapping as shown.

The following formulae show how various factors in the design of the $C_{+/-}$ counter and the adder are determined.

1. Size of fixed number to be added to $C_{+/-}$ counter outputs by adder = $2^n - (12s - 1)$.

   where : 2^n = No. of states of $C_{+/-}$ pulses counter.

   s = summing rate.

   For Summing X1 Added Number = 5
   " " X8 " " = 161
   " " X12 " " = 113
   " " X22 " " = 249

2. Clock rate at pin 22 input to Smoother card.

   = 12 x s x 2.6 kHz,

   where : s = Summing rate.

   2.6 kHz is multiframe frequency.

3. Sizes of adders used in this circuitry.

   Summing X1 = 16 (Max storage controlling capability of 4)
   " X8 = 256 " " " " " 160)
   " X12 = 256 " " " " " 112)
   " X22 = 512 " " " " " 248)

8. SETTING UP MULTIPLEX FOR CORRECT OPERATION

External D.C. supplies are required to power the multiplex. The following supplies are required:

+8V @ approx. 7 A

-15V @ approx. 15 mA

+15V @ approx. 50 mA

The power supplies are connected direct to the plugs at the rear of the unit. The printed circuit cards, accessible by removing the rear cover, are numbered 1 - 15 left to right looking at the rear of the unit. Pin 1 of the connectors is at the bottom.

Looking at the front of the unit the Transmit section of the multiplex is on the left and Receiver Section on the right. Note that they are completely independent. All inputs, except Data-Mux-In, are terminated in approx 100Ω and feed direct to T.T.L. gates. All outputs, except Data-Mux-Out, are buffered by low impedance T.T.L. buffers. The Data-Mux-In and Data-Mux-Out points are designed for 75Ω bipolar levels. The Receiver does not contain any line loss equalisation at the Data-Mux-In point, but it does contain an internal clock extraction circuit, so normally the Clock-Mux-In connector is not used. The transmitter incorporates an internal 8.448 MHz crystal oscillator so normally the Ext connector is not used. The Data and Spare Bit inputs are fed into the Transmitter, via patching points and links for testing purposes. LED's are used to monitor

the states of the Receiver outputs. When the link is removed completely, a low state is continuously sent to the Receiver. When the link is in the upper position a high state is continuously transmitted.

The LED's and shorting links can be used to test whether the multiplex is operating correctly, back-to-back, using the following procedure:

1. Connect power supplies as outlined earlier.

2. Connect a cable from Data-Mux-Out to Data-Mux-In, noting that the "In Sync" LED goes on.

3. Connect a TTL compatible clock at a frequency within 2.048 MHz ± 2.6 kHz into the Ext-Clock-In connector of the channel to be tested. Alternatively one of the Receiver Clock-Outputs can be used as a clock source.

4. Remove the link completely from the channel to be tested and note that the LED corresponding to the same channel on the receiver is off.

5. Place the link in the upper shorting position and note that the LED is on.

The procedure as outlined above can be used for testing each of the 4 channels. The spare bit channels can also be tested the same way. Note that no external clock is provided for the spare channels as the clock rate is internally controlled. The clock rate of each spare channel is 16 kHz and a synchronous clock would need to be derived from the internal counter if the full capacity of the spare channels were to be used. If no synchronous clock is used for the spare channels, it is still possible to transmit data over the spare channels provided that the data rate is lower than about 2 kbit/s. The data offered to the spare channels will be sampled with a 16 kHz clock and the received data will be reconstructed with some jitter, which in the case of 2 kbit/s data will be not more than 12.5%. It is also possible to combine the three spare bit channels to increase the bit rate to 48 kbit/s, which might be used for coded speech with 6 bit coding and 8 kHz sampling.

To send data over the multiplex the shorting link has to be in the lower position.

9. TECHNICAL DATA

9.1 General.

Line pulse rate	8.448 Mbit/s ± 30ppm
Line code	HDB3 (50% duty cycle)
Output voltage of Line pulses	±2.37V ±10% into 75Ω
Type of Multiplexing	Bit Interleaved
No. of frames per multiframe	6
No. of bits per frame	528
Type of Justification System	+/0/-

Frame Synchronisation	Bit Nos. 257-264, with pattern 11101000 once per frame
Average Resynchronisation Time	280μs
Multiframe Synchronisation	Bit No. 521 in each frame, with pattern 110010 spread over 6 frames
Average Resynchronisation Time	1.7ms
Multiplex Frame Structure	Compatibility with synchronous 8.448 Mbit/s multiplex is possible
Justification Codes	+ justification 000111 0 justification 001100 - justification 11000X X = erased bit Majority gating is used in decoding to correct for 1 bit error.
Nominal Justification Rate	0Hz
Justification Capacity	2666.6Hz (nominally)
Clock Option	Ext clock input
Spare Bits	Bits 523, 525, 527 in each frame. Can be used asynchronously in sampling mode.
Capacity	16 kbit/s each
Alarms	Loss of frame or multi-frame synchronisation at local terminal indicated by lamp on front panel

9.2 Tributary Data.

Tributary bit rate	2.048 Mbit/s ± 50ppm
No. of tributaries multiplexed	4
Maximum allowable tributary input jitter	Unlimited for phase change rates below 1750 bit/s.* Approx. 1.2 bit peak-to-peak (586ns) for phase change rates above 1750 bit/s.

* E.g., triangular input jitter with a period P and p-p amplitude δ has a phase change rate of $2P\delta$ bit/s.

Output multiplex jitter of tributary with no input jitter	Maximum of 19% peak to peak (93 ns) over variation of input clock from nominal to ± 160Hz. (With Optional Phase-locked loop 12% p-p).
Input voltage of tributary clock	TTL levels (unipolar clock has to be supplied)
Input impedance of tributary	Approx. 100Ω.

9.3 Line Jitter.

Maximum allowable line jitter on 8.448 Mbit/s line	Unlimited for phase change rates below 2.5 kbit/s. Approx. 0.4 bit peak-to-peak (195 ns) for phase change rates above 2.5 kHz.

10. FINAL REMARKS

The described multiplex has daily operated satisfactorily for almost a year. Several tests, specially on jitter, have been performed. The jitter tests are reported in R.L. Report No. 6941. In the first two months of operation three integrated circuits became faulty : an adder, an elastic store and a gate. No further integrated circuit faults have occurred.

As explained in sections 5.1 and 6.4 some design modifications were necessary for the cascading of a synchronous counter and the clocking of asynchronous data with a Schottky J-K flip-flop. In both cases the conditions under which the components were operating were not fully specified in the manufacturers data handbook.

The Smoother card (Cct 8) could be replaced with a custom designed I.C. This card works with pulse rates below 100 kHz and because of its large degree of repetition is very suitable for integration. A circuit in MOS or C-MOS techniques would be the obvious choice.

The circuitry for +/0/- justification is slightly more complicated than for positive justification. It is estimated that about 10-20% more components are required for +/0/- justification than for positive justification using the design in this report. In contrast herewith, S.T.C. states that approximately 40% more components are required using their design (Ref. 5, p.91). The quoted 10-20% does not take into account the smoothing circuits required for positive or +/0/- justification. With a custom I.C. for the smoother, the number of components required for smoothing would compare favourably with an ordinary phase-locked loop normally used with positive justification.

Advantages of +/0/- justification over positive justification are given in References 6 and 7.

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5. Jessop, A., Norman, P., Waters, D.B., "120-Megabit per Second Coaxial System Demonstrated in the Laboratory", Electrical Communication, Vol. 48, Nos. 1 and 2, pp.79-92, 1973.

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7. Bylstra, J.A., "Asychronous Multiplexing with Positive-Zero-Negative Justification", IREE (Australia) National Convention Digest, pp.214-215, August 1973.

APPENDIX I

AIDS IN TROUBLE SHOOTING

The following aids in trouble shooting are of assistance for location of a fault in the multiplex.

To assist in fault location some cards are provided with test pins located at the rear of the card. The pins are numbered, and pin no. 1 of a particular card is at the bottom.

Fault finding should always commence by checking supply voltages. Faults in the transmitter and receiver may be localised by examining waveforms at appropriate points. Some waveforms are shown in the attached figures and drawings. A handy oscilloscope triggering point for most waveforms is the pulse occurring at multiframe rate. This pulse is available on test pin 1 of card 14.

1.1 Transmitter. The following list gives some main points to check in localising a fault in the transmitter.

1. Check that the 8.448 MHz oscillator is operating and of correct frequency. i.e., 8.448 MHz ± 30 ppm.

2. Check that the Frame and Multiframe counter is operating correctly by checking waveforms with figure 3.

3. The Elastic Store and Phase Detector cards are provided with test pins connected to the read and write clocks. If the justification process is operating correctly these frequencies should on average be equal. This can be checked with an average reading counter. The Elastic Store and Phase Detector for channels 1 and 3 are on card 13, and for channels 2 and 4 on card 12. For the channel numbers 1 and 3 test pin 1 is the write clock, and pin 2 is the read clock. For channel numbers 2 and 4 the pin numbers are 3 and 4 respectively.

4. Test pin 2 on card 14 can be used to monitor the multiplexed data output (unipolar) and check that multiplexing, code generation, etc., is correct.

1.2 Receiver. The following list gives some main points to check in localising a fault in the receiver.

1. Check frame and multiframe synchronisation (lamp at front panel, in sync = lamp is on).

2. Check that the extracted 8.448 MHz clock is locked to the transmitter clock. If it is not locked coil L1 may need retuning.

3. Check that the 24.576 MHz clock is locked in correctly to the transmitter. This can be checked by triggering an oscilloscope at multiframe rate, and viewing the 24.576 MHz clock, which is available at test pin 1 on card 1. The waveform should be clean and steady. If it is not locked in, potentiometer P1 (above test pin 1) may need readjustment.

4. To check that the command information is being decoded correctly, the frequency of the buffer write clock can be measured. Test pin 4 on the Buffer - Smoother card is connected to the write clock of the buffer. This frequency and the transmitter input clock frequency should on average be equal, which can be checked using a counter.

5. Test pin 2 on the Buffer - Smoother card is connected to the smoothed clock output; its frequency and the transmitter input clock frequency should be equal. One way to check that they are equal is to use an oscilloscope. Note that at low justification rates the jitter on the smoothed clock should be approximately 9% p-p.

6. To check that the smoother is operating correctly the frequency of the $C_{+/-}$ pulses can be measured. If the smoother is operating correctly the frequency of the $C_{+/-}$ pulses will be on average 12 times the command rate (justification rate). On the Buffer-Smoother card test pin 1 is connected to the $C_{+/-}$ pulse stream. Using a counter the frequency of the signal on test pin 2 is compared with the frequency of the C_+ or C_- outputs of the particular channel on the gating card. Alternatively, if the justification rate is known it is possible to check that the $C_{+/-}$ pulse rate on test pin 2 is 12 times the known justification rate.

APPENDIX II

Changes for operation at Input Tributary Bit Rates other than 2.048 Mbit/s.

It is relatively easy to change the multiplex for operation at input bit rates up to 2.048 Mbit/s. The changes to be made are listed below.

1. Change crystal frequency in the transmitter according to the following formula. Note that the crystal is working in parallel mode.

$$f_s = \frac{33}{8} f_p$$

where: f_s = Multiplex frequency

f_p = Incoming tributary bit rate.

2. In the receiver (Cct 4), clock extracting coil (L1) primary inductance has to be changed to resonate with 33pF at the multiplex frequency. It is essential that the turns ratio of L1 remains the same. Refer to Mullard Technical Handbook, book 3, for data on the particular Vinkor used.

3. The time duration of the monostables used for frame and multiframe synchronisation in the receiver has to be modified (see Cct 5). Formulae are given in the TTL Data Book for calculating timing components.

   1. D3(12) should be 20% longer than 1 frame period.

   2. D3(13) should be 20% longer than 4 frame periods.

   3. E1(13) should be 20% longer than 4 multiframe periods (24 frame periods).

   Duration of 1 frame $= \frac{528}{f_s}$

   where : f_s = Multiplex frequency.

4. The crystal frequency in the PLL used for generating the smoothing clock has to be changed to be 12 times the input tributary frequency (Cct 4). D1(2) and associated components form the crystal oscillator, with L2 and C9 forcing the crystal to work in an overtone mode. L2 and C9 may need readjustment when the crystal frequency is other than 24.576 MHz. Note that the crystal is working in series mode.

   For optimum operation of the PLL, R13, 14, 15, 16 and C5 (Cct 4) may need readjustment. PLL parameters are given in the circuit description.

5. For operation at input tributary rates of less than 1.5 MHz the time duration of monostable D5(12), Cct 7, may need to be increased. D5(12) generates the load pulse from the positive edge of the smoother latch pulse. The load pulse must be a minimum of 50 ns longer than the Smoother Latch pulse.

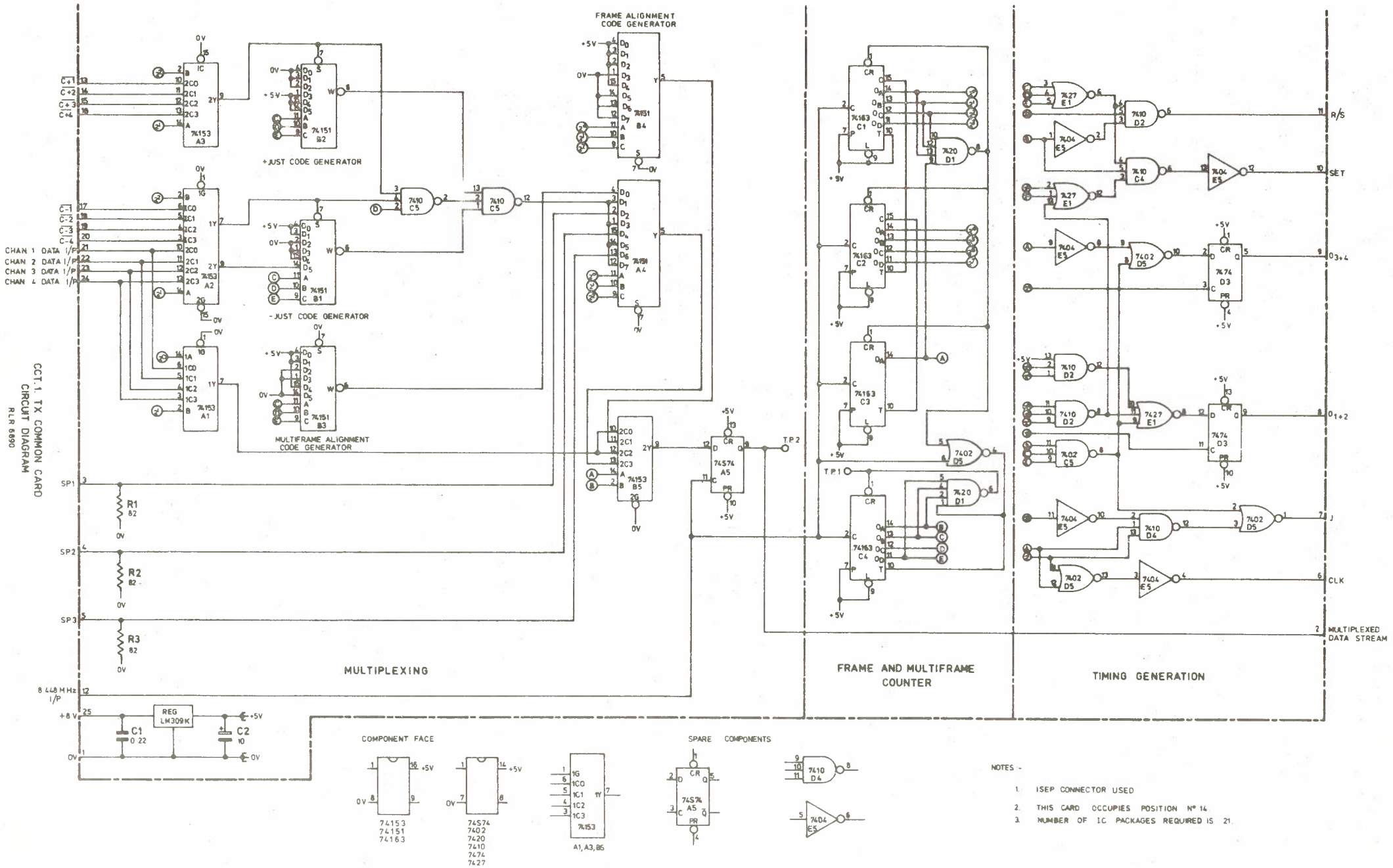
LIST OF INTEGRATED CIRCUITS USED

1. SN7400N - 4 x 2 i/p Nand gate
2. SN74S00N - 4 x 2 i/p Nand gate. (Schottky)
3. SN7402N - 4 x 2 i/p Not gate.
4. SN7403N - 4 x 2 i/p Nand gate. Open collector.
5. SN7404N - Hex invertor.
6. SN74S04N - Hex invertor. (Schottky).
7. SN7408N - 4 x 2 i/p And gate.
8. SN7410N - 3 x 3 i/p Nand gate.
9. SN7411N - 3 x 3 i/p And gate.
10. SN7412N - 3 x 3 i/p Nand gate. Open collector.
11. SN7420N - 2 x 4 i/p Nand gate.
12. SN74S20N - 2 x 4 i/p Nand gate (Schottky).
13. SN74H21N - 2 x 4 i/p And gate (High Speed)
14. SN7427N - 3 x 3 i/p Not gate.
15. SN7430N - 1 x 8 i/p Nand gate.
16. SN7438N - 4 x 2 i/p Nand power gate (Open Collector).
17. SN7442N - B.C.D. to Decimal Decoder.
18. SN74H55N - Expandable 4 i/p And-Or-Invert gate.
19. SN74H60N - 2 x 4 i/p Expander.
20. SN7473N - Dual JK Master-Slave flip flop.
21. SN7474N - Dual D type flip flop. Edge triggered.
22. SN74S74N - Dual D type flip flop. Edge triggered. (Schottky).
23. SN7483N - 4 bit full Adder.
24. SN74LS83N - 4 bit full Adder (Low power Schottky).
25. SN7485N - 4 bit Comparator.
26. SN7486N - 4 x 2 i/p Exclusive Or gate.
27. SN7493N - 4 bit Counter, Asynchronous.
28. SN74111N - Dual J.K. Master-Slave flip flop with Data Lockout.
29. SN74S113N - Dual J.K. flip flop, Neg. Edge Triggered (Schottky).
30. SN74S114N - Dual J.K. flip flop, Neg. Edge Triggered (Schottky).
31. SN74123N - Dual Monostable Multi-vibrators, Retriggerable, Resettable.
32. SN74151N - 1 out of 8 bit Data Selector.
33. SN74153N - Dual 1 out of 4 bit Data Selectors.
34. SN74155N - Dual, 2 bit Binary to 1 of 4 Decoder, Demultiplexer.
35. SN74161N - 4 bit Binary Counter, Synchronous. Asynchronous clear.
36. SN74163N - 4 bit Binary Counter, Fully Synchronous.
37. SN74175N - Quad D type flip flop.

38. 93L16 - 4 bit Binary Counter. Synchronous. Asynchronous clear (Low Power).
39. 9338 - 8 bit Multiple Port Register.
40. DM8830 - Dual Differential Line Driver.
41. MC4044 - Phase-Frequency Detector.
42. LM308 - Operational Amplifier.
43. µA760 - High Speed Differential Comparator.
44. LM309K - +5V Regulator.
45. LM309H - +5V Regulator.
46. LM320H - -5.2V Regulator.
47. TBA625 - +12V Regulator.

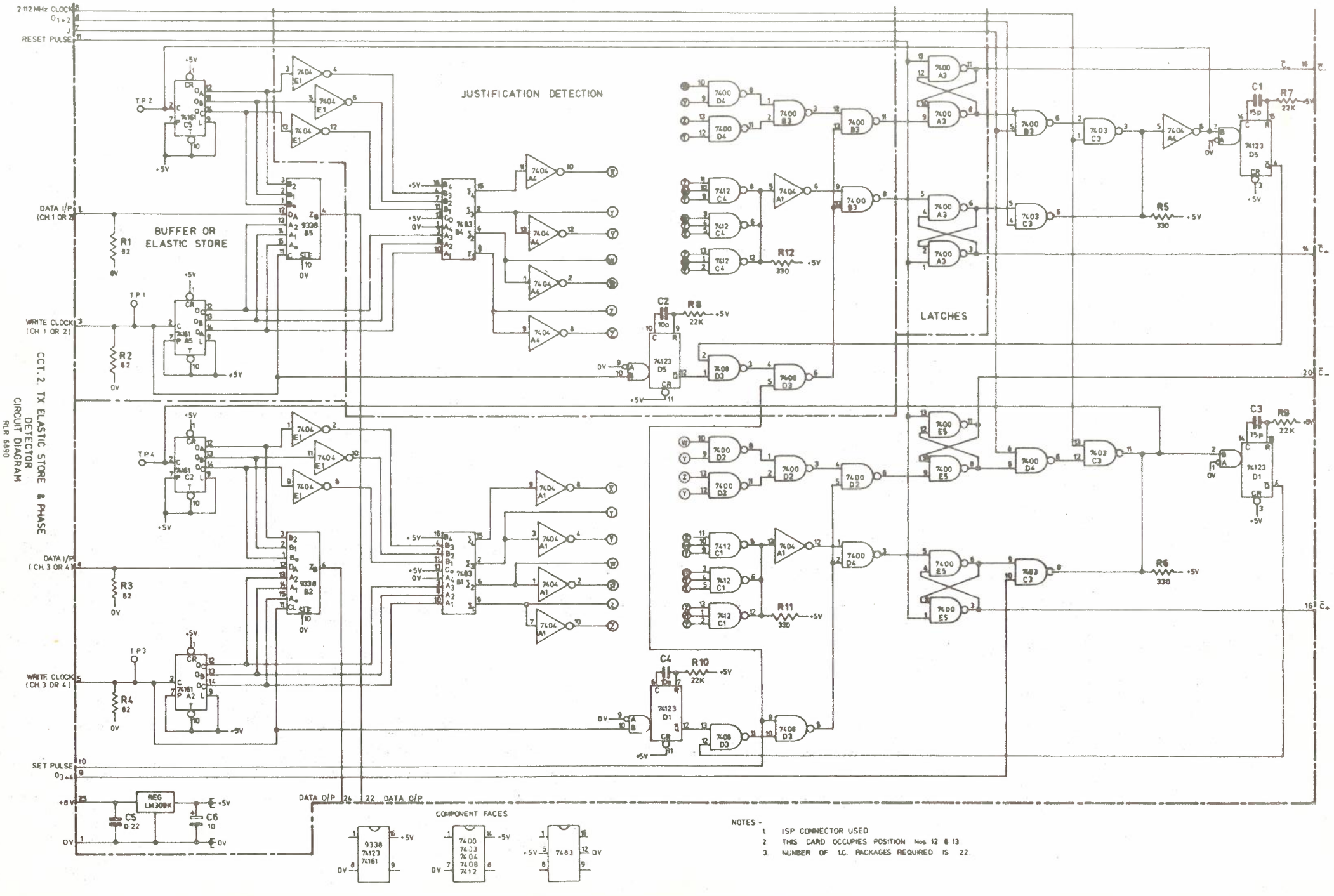
List of Figures

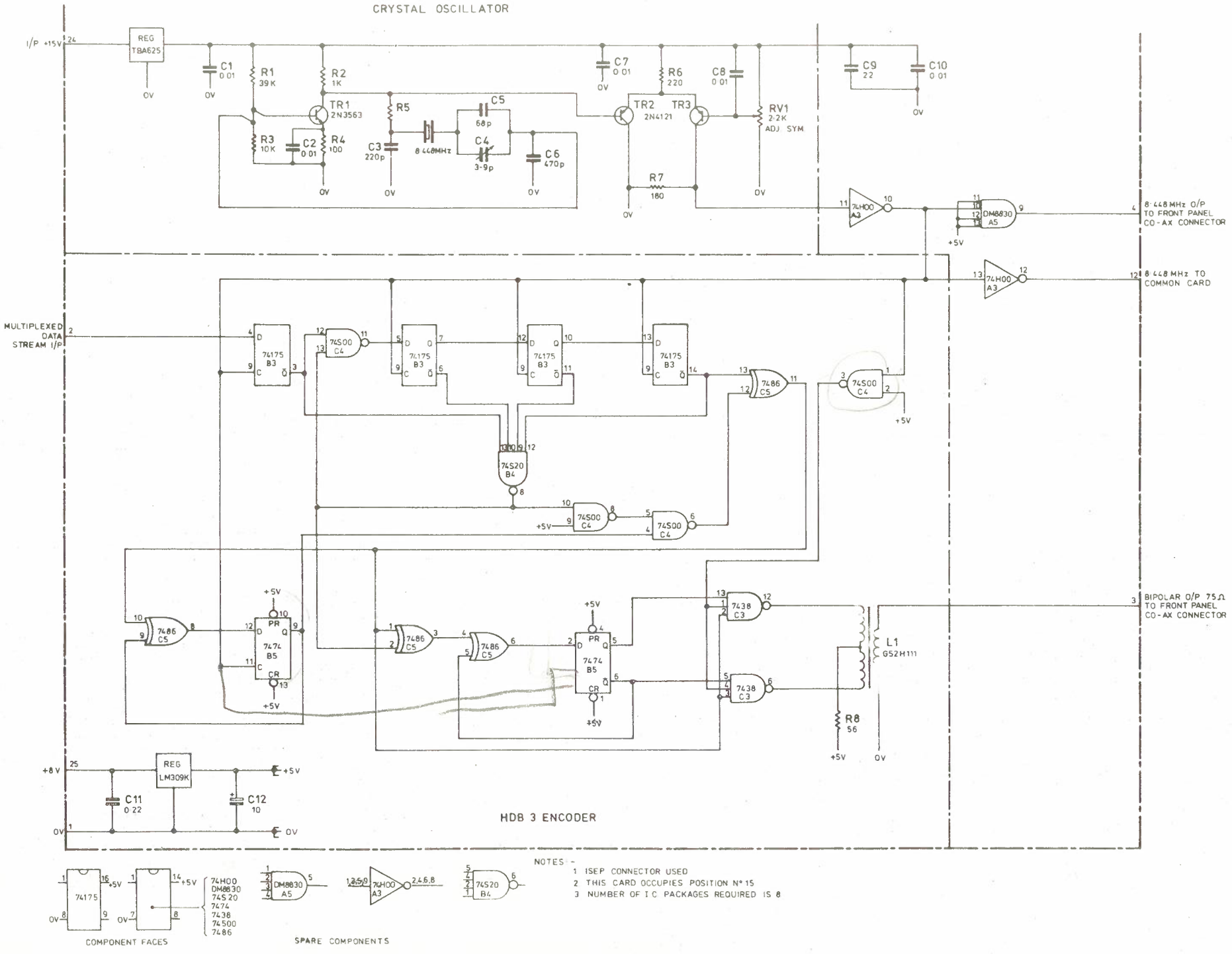
List of Circuit Drawings



NOTES :-

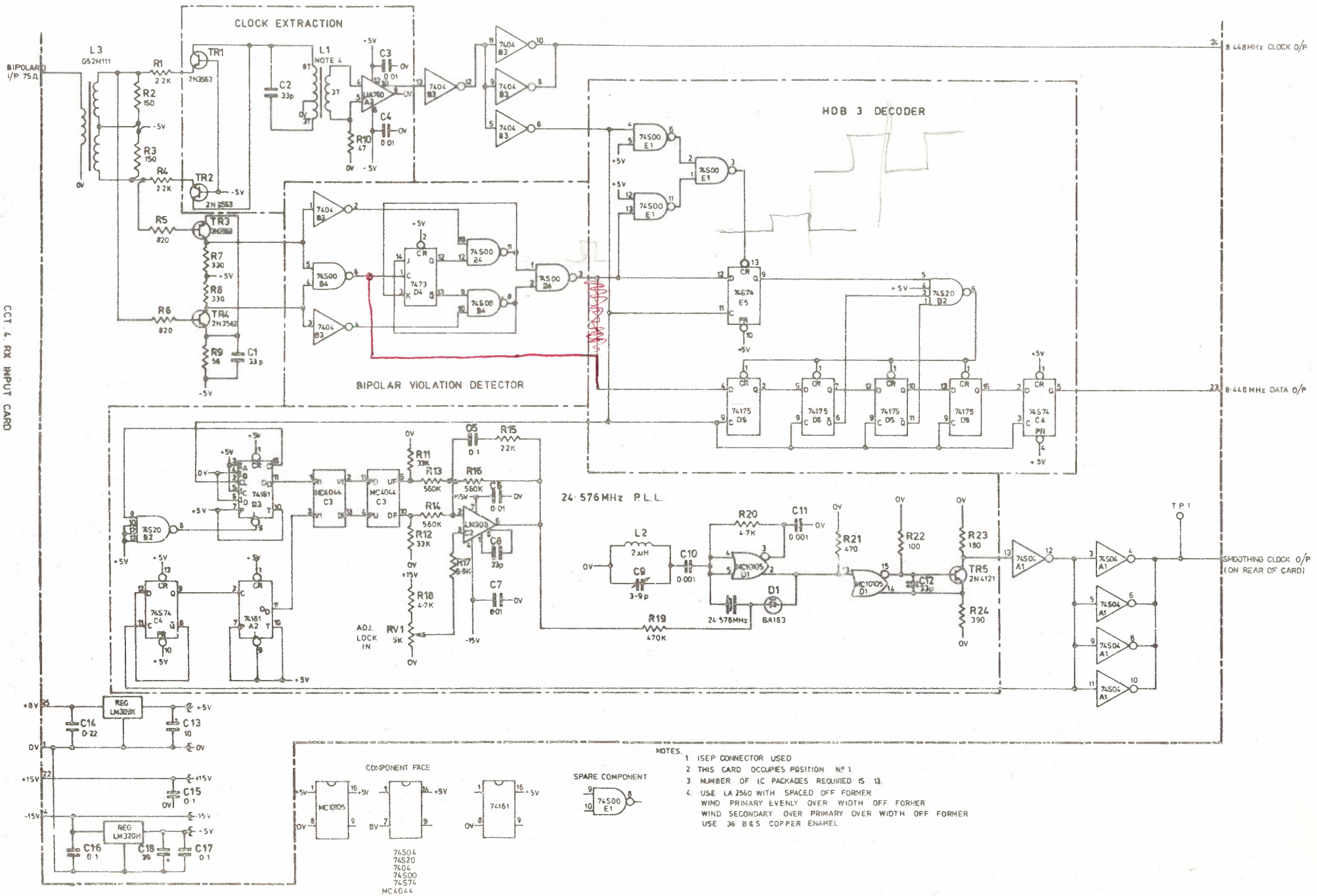
1. ISEP CONNECTOR USED
2. THIS CARD OCCUPIES POSITION N° 14
3. NUMBER OF IC PACKAGES REQUIRED IS 21

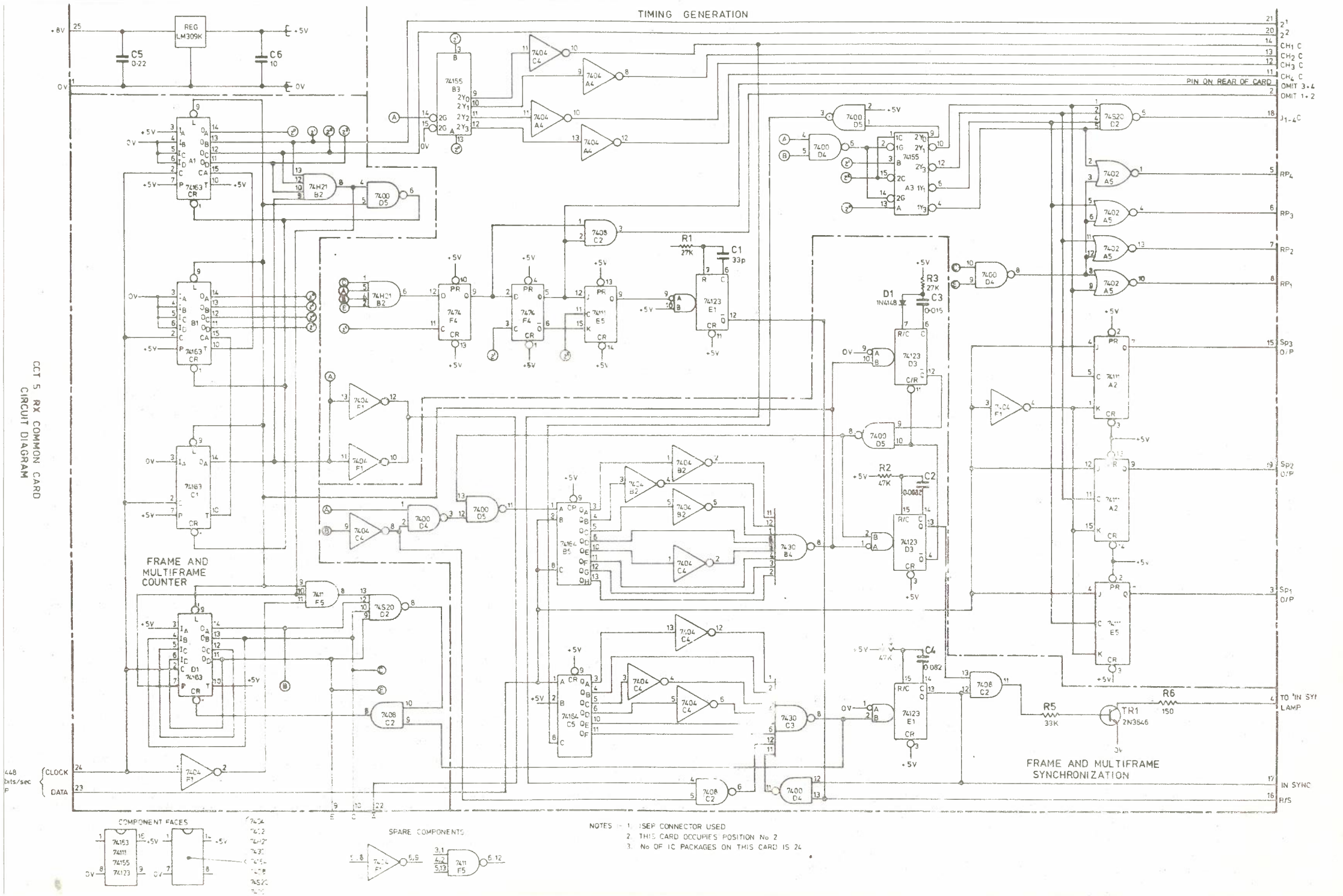

CCT. 2. TX ELASTIC STORE & PHASE DETECTOR CIRCUIT DIAGRAM
RLR 6890
2.112 MHz CLOCK
RESET PULSE
JUSTIFICATION DETECTION
BUFFER OR ELASTIC STORE
DATA I/P (CH.1 OR 2)
WRITE CLOCK (CH.1 OR 2)
DATA I/P (CH.3 OR 4)
WRITE CLOCK (CH.3 OR 4)
SET PULSE
LATCHES
TP1
TP2
TP3
TP4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
C1
C2
C3
C4
C5
C6
REG LM309K
DATA O/P
DATA O/P
COMPONENT FACES
NOTES -
1 ISP CONNECTOR USED
2 THIS CARD OCCUPIES POSITION Nos 12 & 13
3 NUMBER OF I.C. PACKAGES REQUIRED IS 22

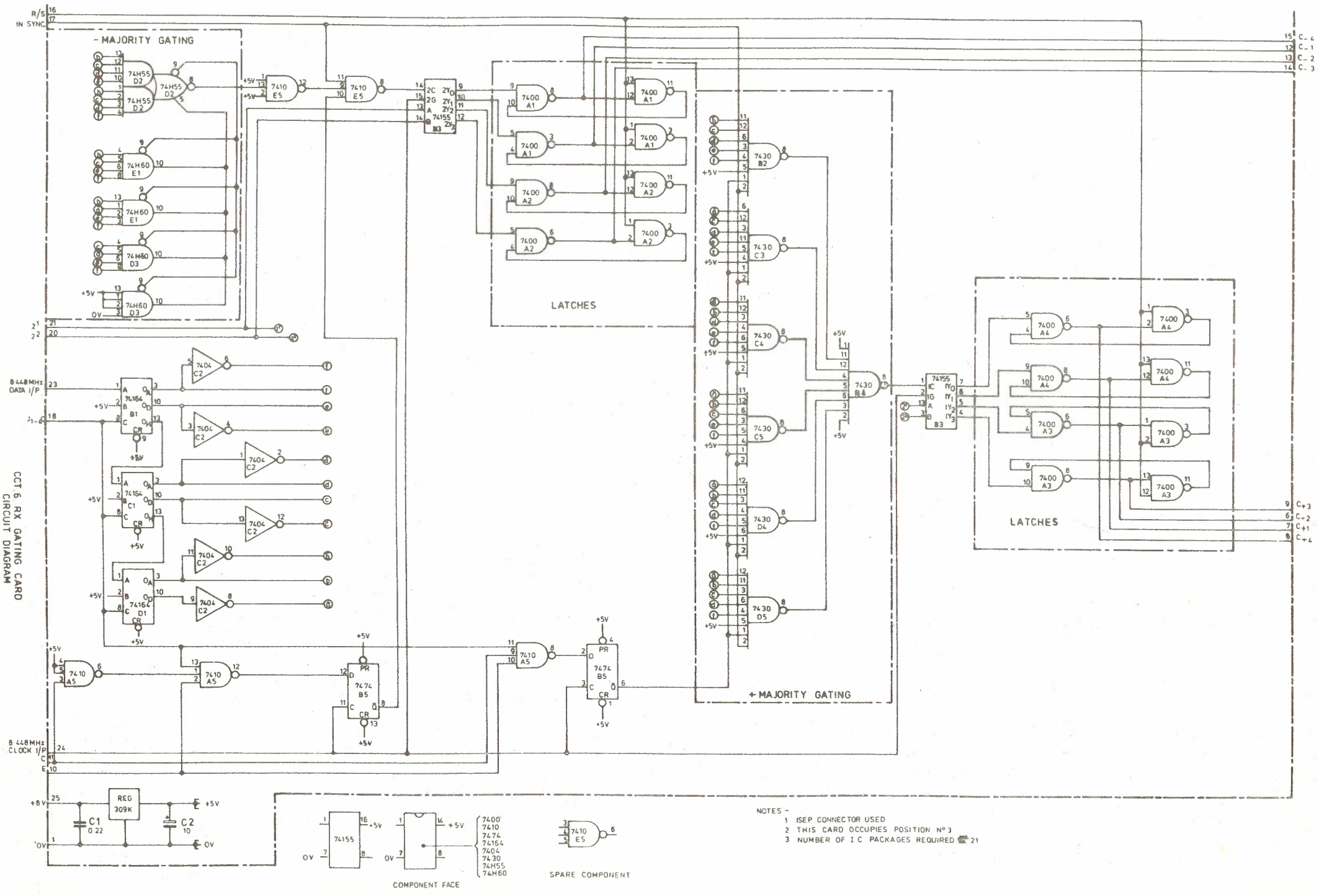


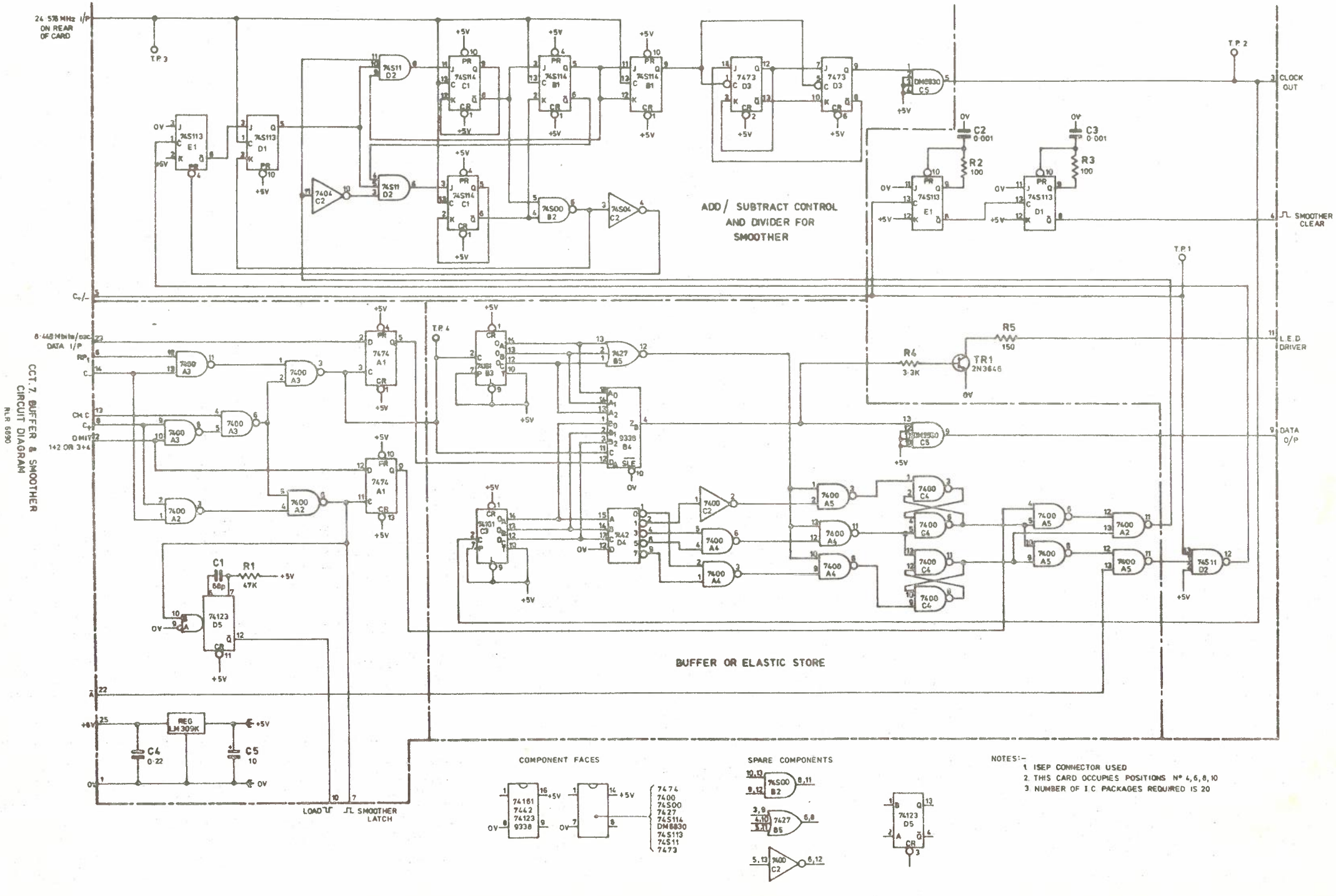
NOTES -

1 ISEP CONNECTOR USED
2 THIS CARD OCCUPIES POSITION N° 15
3 NUMBER OF I C PACKAGES REQUIRED IS 8


CCT. & RX INPUT CARD
CIRCUIT DIAGRAM
RLR 6990
CLOCK EXTRACTION
BIPOLAR I/P 75Ω
L3
GS2H111
R1 2·2K
R2 150
R3 150
R4 2·2K
R5 820
R6 820
R7 330
R8 330
R9 56
C1 33p
TR1 2N3563
TR2 2N3563
TR3
TR4 2N3563
L1 NOTE 4
C2 33p
C3 0·01
C4 0·01
R10 47
LM360 A2
7404 B3
BIPOLAR VIOLATION DETECTOR
7473 D4
74S00 B4
74S08 B4
HDB 3 DECODER
74S00 E1
74S20 B2
74S74 E5
74175 D5
74175 D6
74175 D7
74175 D8
74S74 C4
8·448MHz CLOCK O/P
8·448MHz DATA O/P
24·576MHz P.L.L.
74161 B3
74161 A2
74S74 C4
MC4044 C3
LM308 C2
R11 39K
R12 33K
R13 560K
R14 560K
R15 22K
R16 560K
R17 56K
R18 4·7K
R19 470K
RV1 5K
ADJ. LOCK IN
C5 0·1
C6 33p
C7 0·01
C8 0·01
L2 2μH
C9 3-9p
C10 0·001
C11 0·001
C12 33p
R20 4·7K
R21 470
R22 100
R23 180
R24 390
MC10105 D1
24·576MHz
BA183
TR5 2N4121
74S04 A1
TP1
SMOOTHING CLOCK O/P (ON REAR OF CARD)
REG LM309K
REG LM320H
C13 10
C14 0·22
C15 0·1
C16 0·1
C17 0·1
C18 10
COMPONENT FACE
MC10105
74161
74S04
74S20
7404
74S00
74S74
MC4044
SPARE COMPONENT
74S00 E1
NOTES.
1. ISEP CONNECTOR USED
2. THIS CARD OCCUPIES POSITION Nº 1.
3. NUMBER OF IC PACKAGES REQUIRED IS 13.
4. USE LA 2560 WITH SPACED OFF FORMER
WIND PRIMARY EVENLY OVER WIDTH OFF FORMER
WIND SECONDARY OVER PRIMARY OVER WIDTH OFF FORMER
USE 36 B&S COPPER ENAMEL

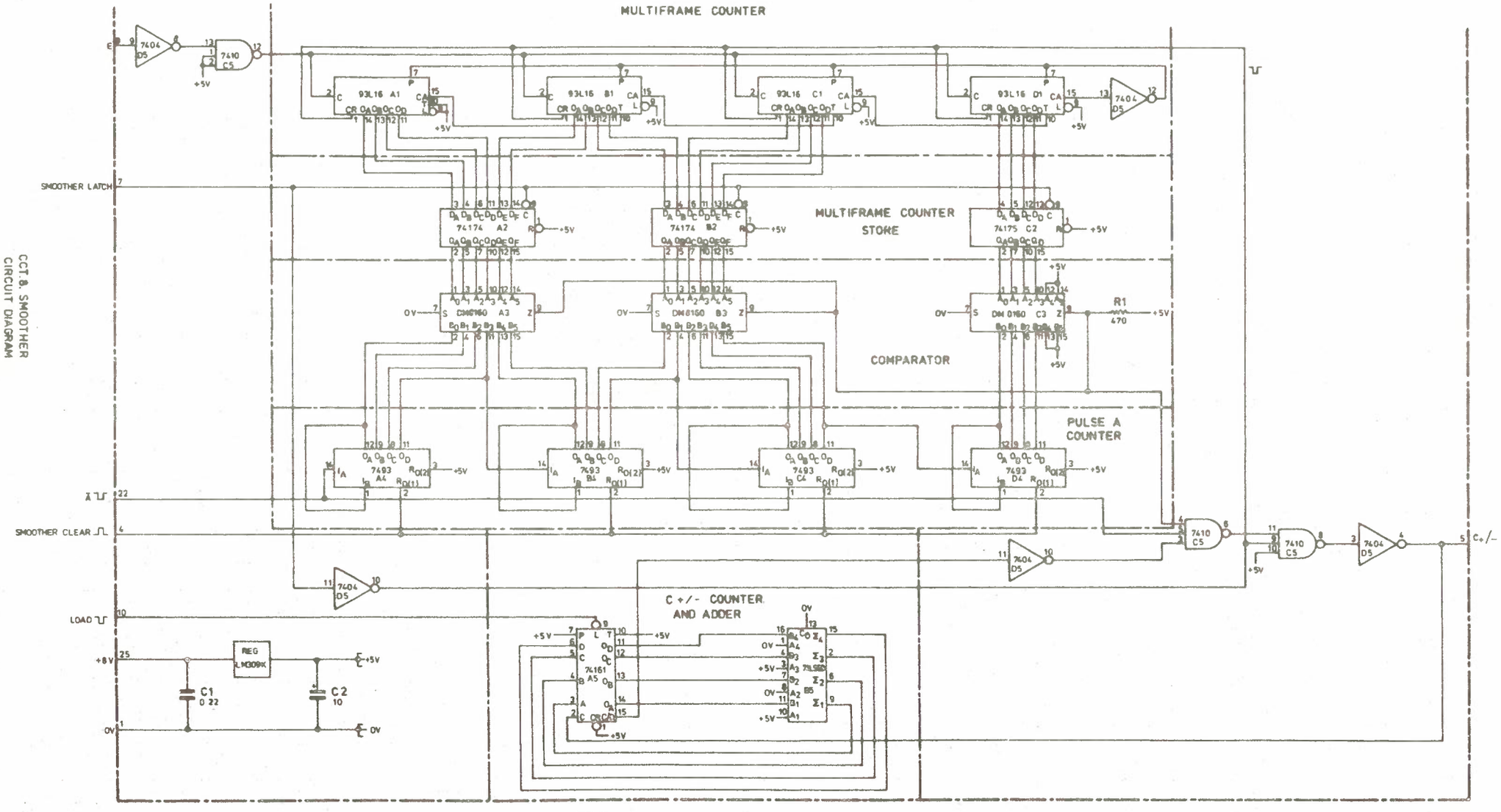

CCT 5 RX COMMON CARD
CIRCUIT DIAGRAM
TIMING GENERATION
FRAME AND MULTIFRAME COUNTER
FRAME AND MULTIFRAME SYNCHRONIZATION
PIN ON REAR OF CARD
CLOCK
DATA
448 bits/sec
IN SYNC
R/S
TO 'IN SYNC' LAMP
COMPONENT FACES
SPARE COMPONENTS
NOTES :- 1. ISEP CONNECTOR USED
2. THIS CARD OCCUPIES POSITION No 2
3. No OF IC PACKAGES ON THIS CARD IS 24

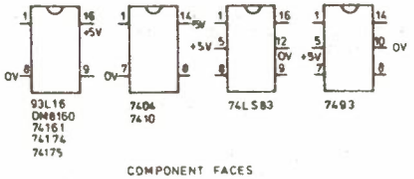

R/S IN SYNC
- MAJORITY GATING
74H55 D2
74H60 E1
74H60 D3
7410 E5
2C 2G A B 74155 B3
LATCHES
7400 A1
7400 A2
7430 B2
7430 C3
7430 C4
7430 C5
7430 D4
7430 D5
7430 B4
74155 B3
+ MAJORITY GATING
LATCHES
7400 A4
7400 A3
8·448MHz DATA I/P
8·448MHz CLOCK I/P
74164 B1
74154 C1
74164 D1
7404 C2
7410 A5
7474 B5
PR CR
REG 309K
C1 0·22
C2 10
+8V
+5V
0V
C-4
C-1
C-2
C-3
C+3
C+2
C+1
C+4
CCT 6. RX. GATING CARD CIRCUIT DIAGRAM
RLR 5890
COMPONENT FACE
7400
7410
7474
74164
7404
7430
74H55
74H60
SPARE COMPONENT
NOTES -
1 ISEP CONNECTOR USED
2 THIS CARD OCCUPIES POSITION N° 3
3 NUMBER OF I C PACKAGES REQUIRED 21


24·576 MHz I/P ON REAR OF CARD
T.P.3
T.P.2
CLOCK OUT
ADD / SUBTRACT CONTROL AND DIVIDER FOR SMOOTHER
SMOOTHER CLEAR
T.P.1
T.P.4
8·448 Mbits/sec DATA I/P
L.E.D. DRIVER
DATA O/P
BUFFER OR ELASTIC STORE
LOAD
SMOOTHER LATCH
CCT.7. BUFFER & SMOOTHER CIRCUIT DIAGRAM
RLR 6690
COMPONENT FACES
SPARE COMPONENTS
NOTES:-
1. ISEP CONNECTOR USED
2. THIS CARD OCCUPIES POSITIONS N° 4, 6, 8, 10
3. NUMBER OF I.C PACKAGES REQUIRED IS 20

CCT.8. SMOOTHER CIRCUIT DIAGRAM

RLR 6890





COMPONENT FACES

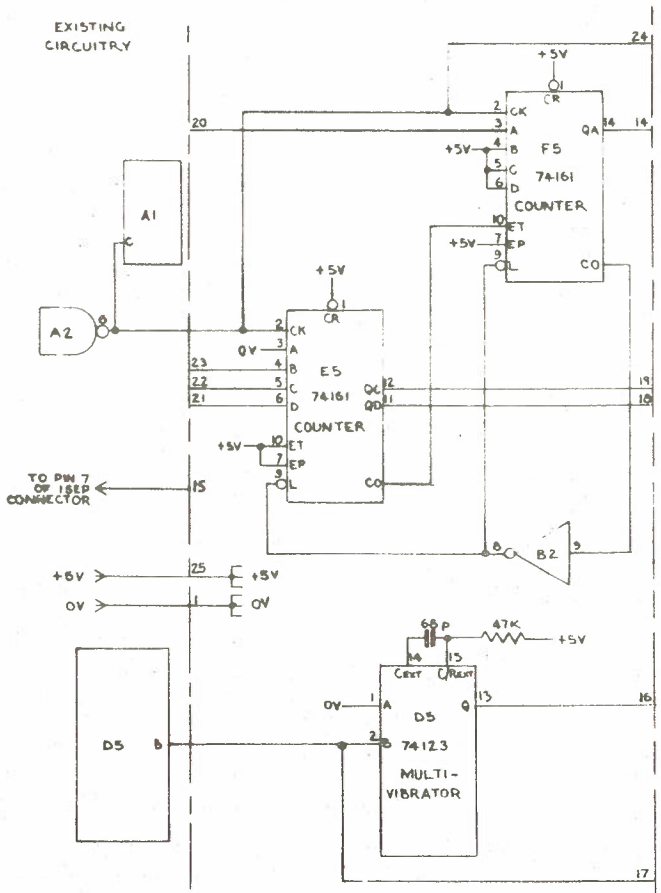
NOTES:-

1. ISEP CONNECTOR USED
2. THESE CARD OCCUPIES POSITION Nos 5,7,9,11 E.G. 4 SIMILAR CARDS
3. NUMBER OF I.C. PACKAGES REQUIRED IS 18

CCT. 9. MODIFICATIONS FOR SUMMING CIRCUIT DIAGRAM

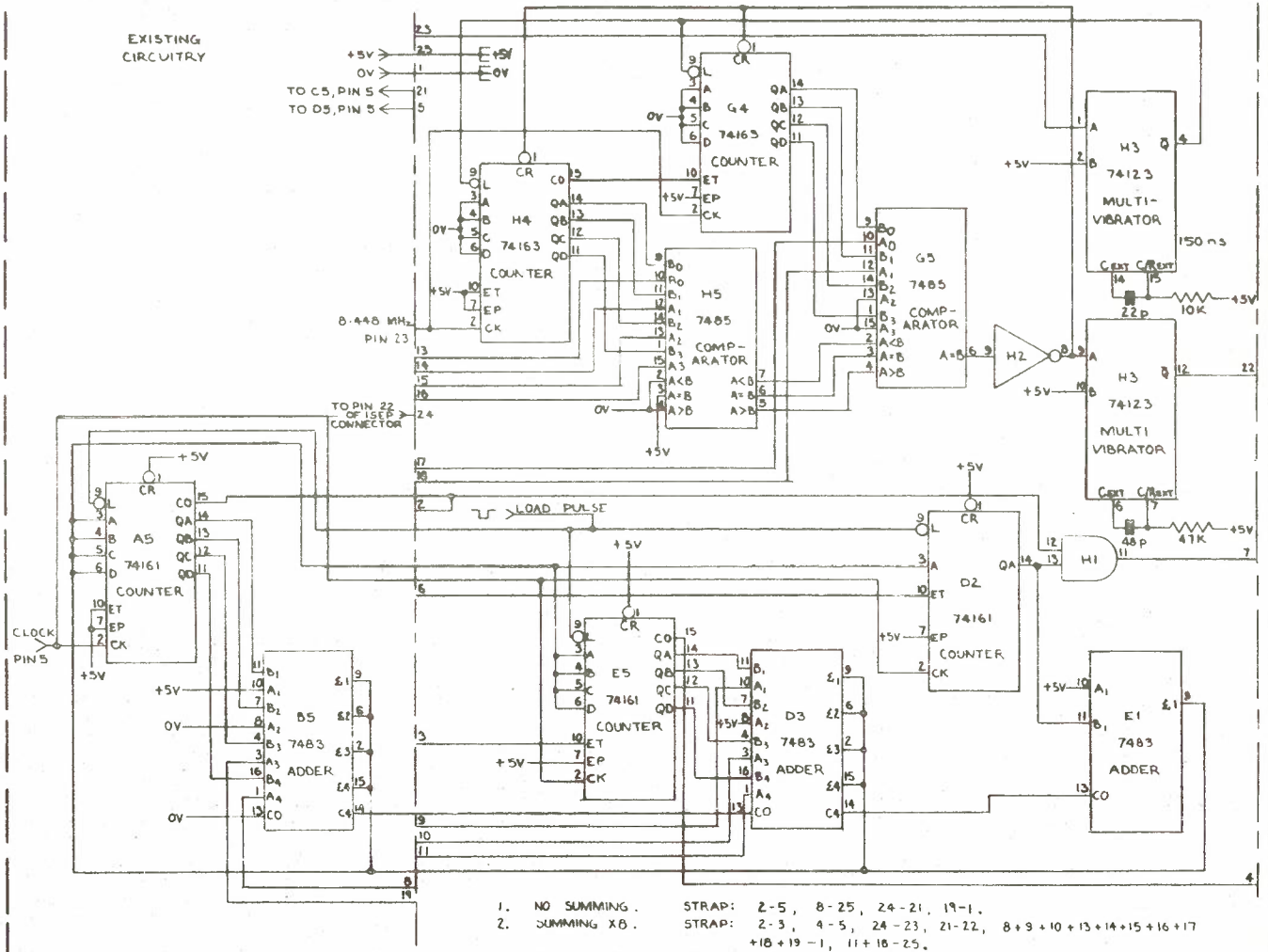
RLR 6990

MODIFICATIONS TO BUFFER CARD (R_X)



1. NO SUMMING. STRAP: 24 + 17 + 15.
2. SUMMING X8 STRAP: 20 + 21 − 25, 22 + 23 − 1, 19 − 17, 16 − 15.
3. SUMMING X12 STRAP: 23 + 21 − 1, 22 + 20 − 25, 18 − 17, 16 − 15.
4. SUMMING X22 STRAP: 23 + 21 − 25, 22 + 20 − 1, 14 − 17, 16 − 15.

MODIFICATIONS TO SMOOTHER CARD (R_X)



1. NO SUMMING. STRAP: 2-5, 8-25, 24-21, 19-1.
2. SUMMING X8. STRAP: 2-3, 4-5, 24-23, 21-22, 8+9+10+13+14+15+16+17+18+19−1, 11+18−25.
3. SUMMING X12. STRAP: 2-3, 4-5, 21-22, 23-24, 8+11+14+16+18+19−1, 9+10+13+15+17−25.
4. SUMMING X22. STRAP: 2-3, 4-6, 7-5, 24-23, 21-22, 8+15+17+18−1, 9+10+11+13+14+16+19−25.

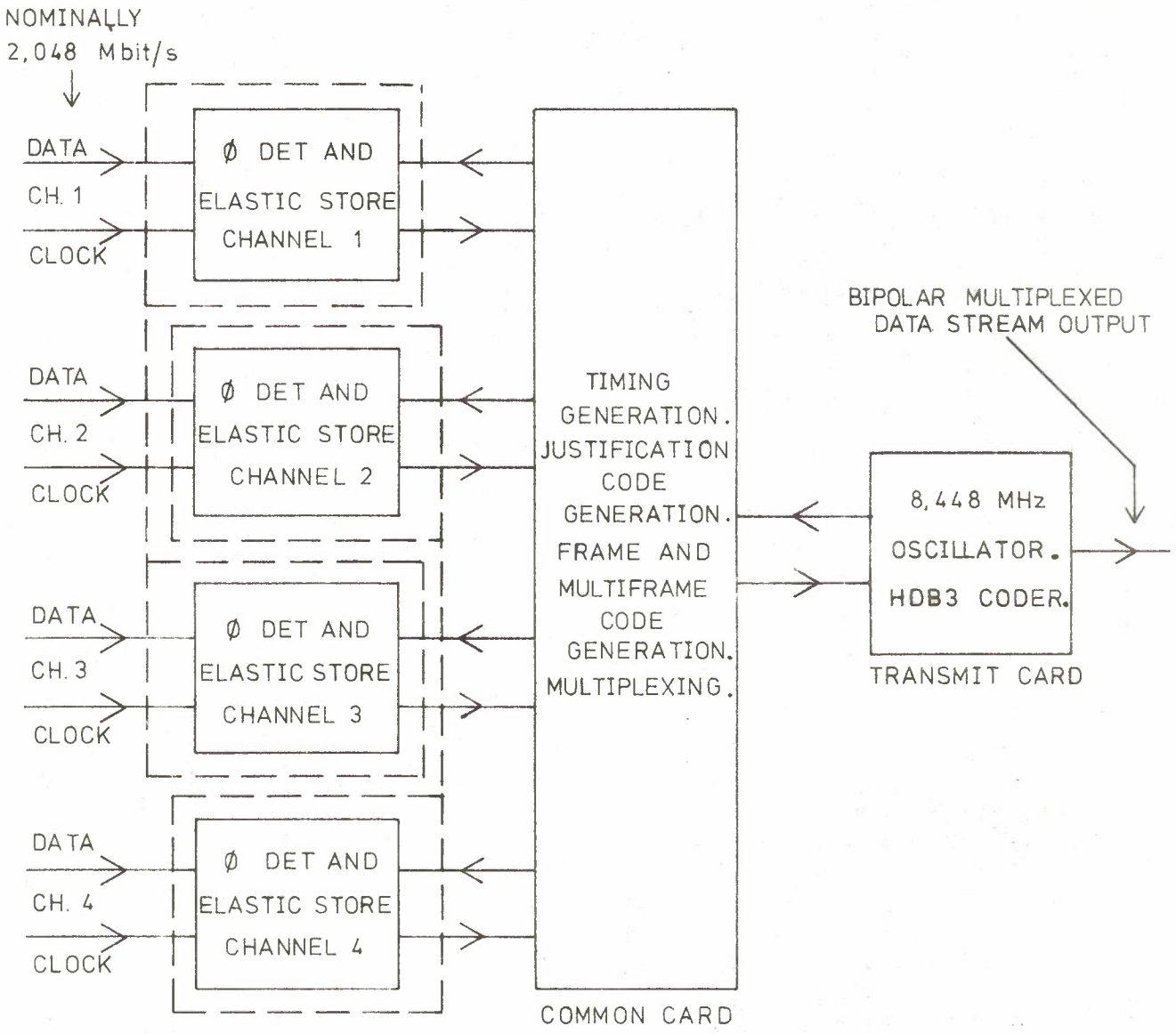


FIG. 1 BLOCK DIAGRAM TRANSMITTER.

6890

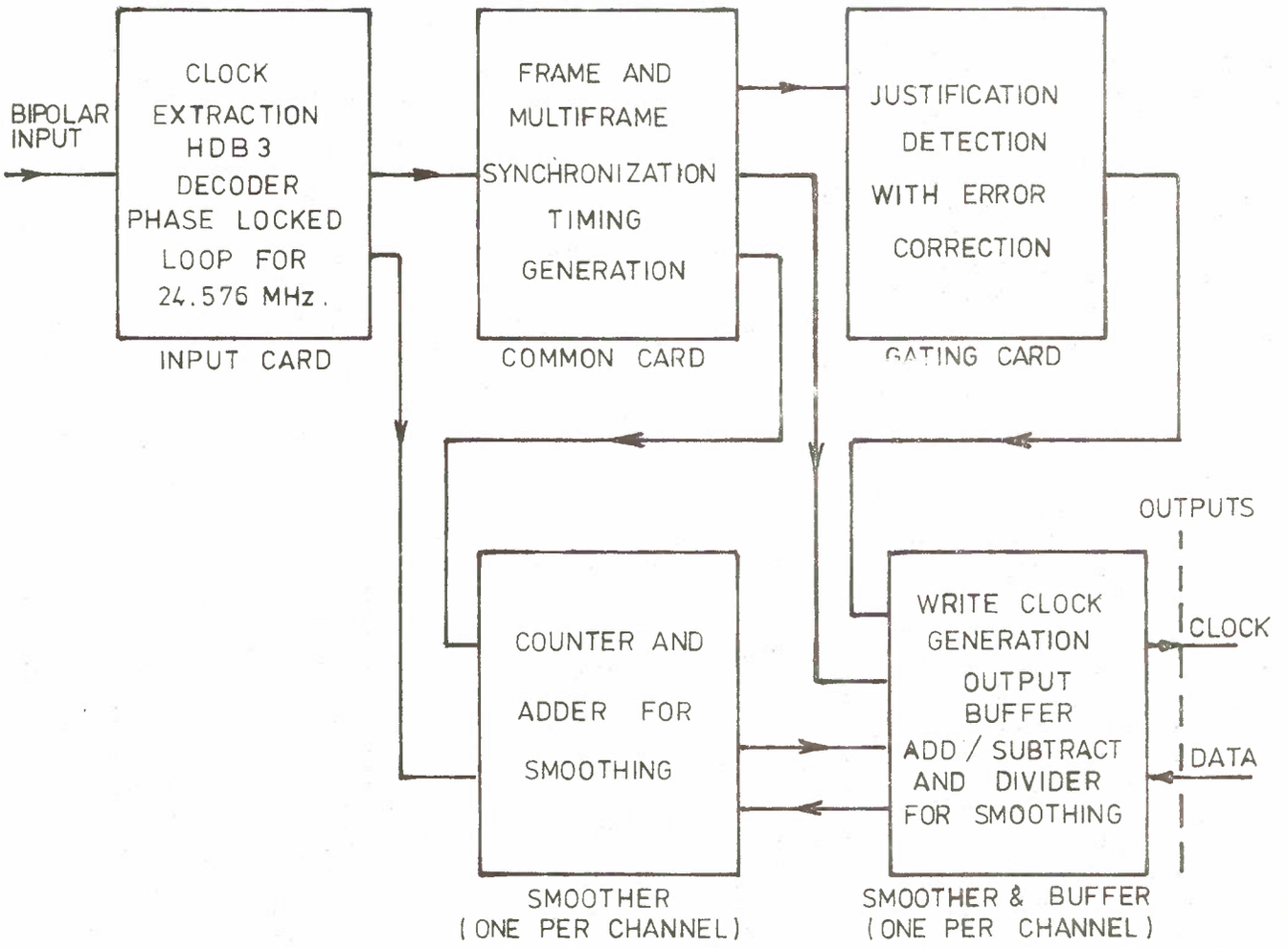


FIG. 2. BLOCK DIAGRAM RECEIVER

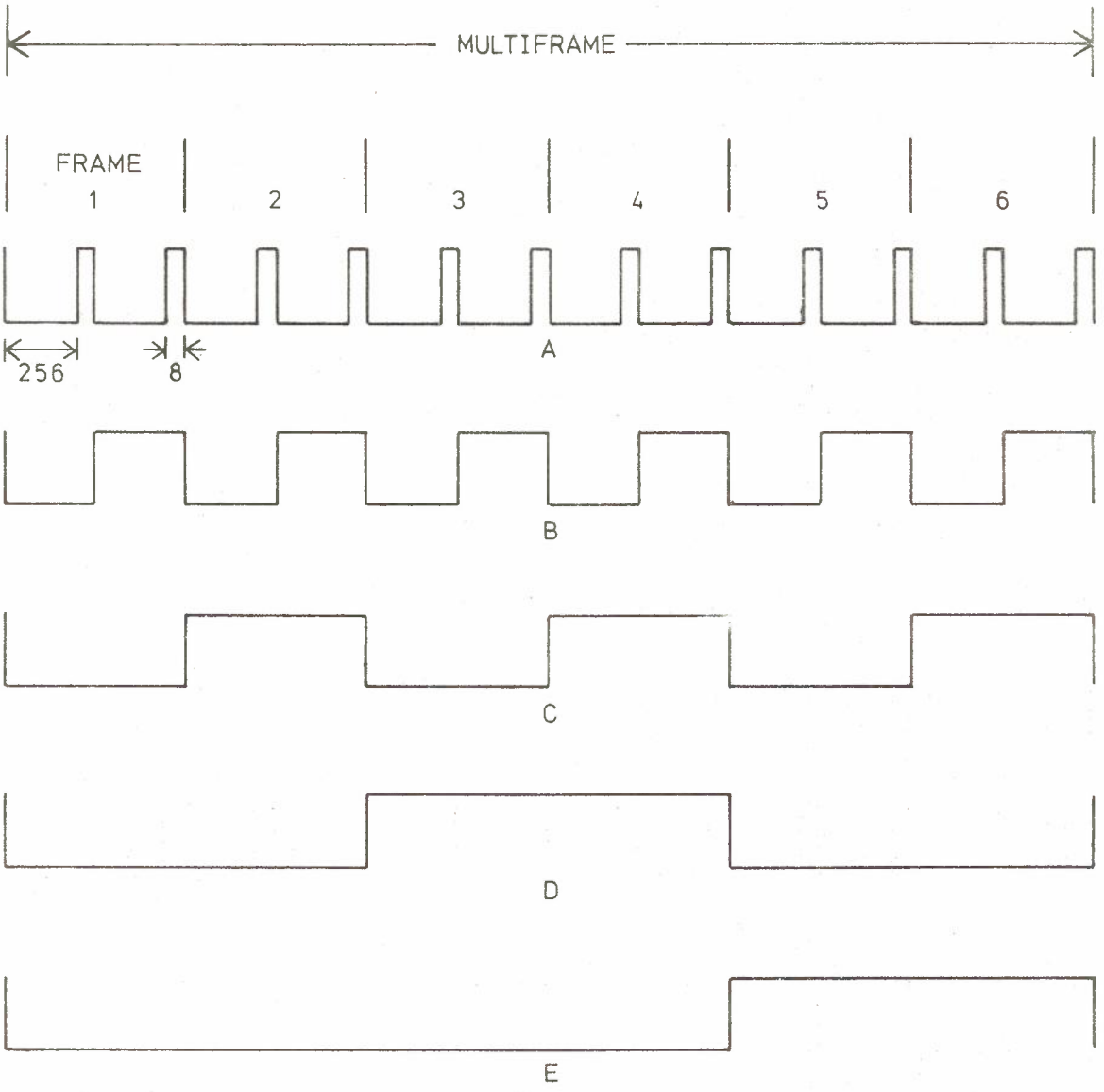


FIG. 3 COMMON CARD TIMING (TRANSMITTER)

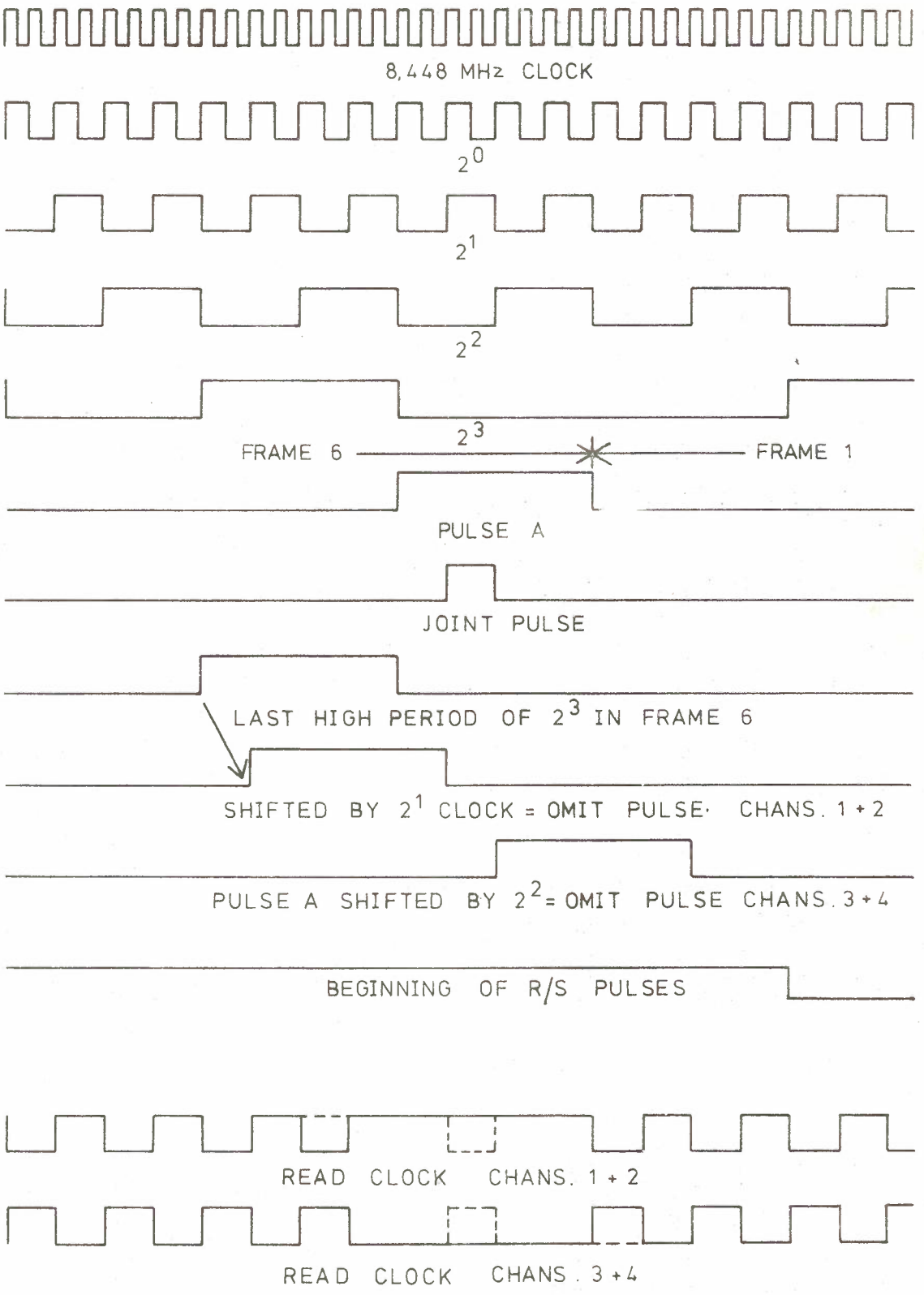
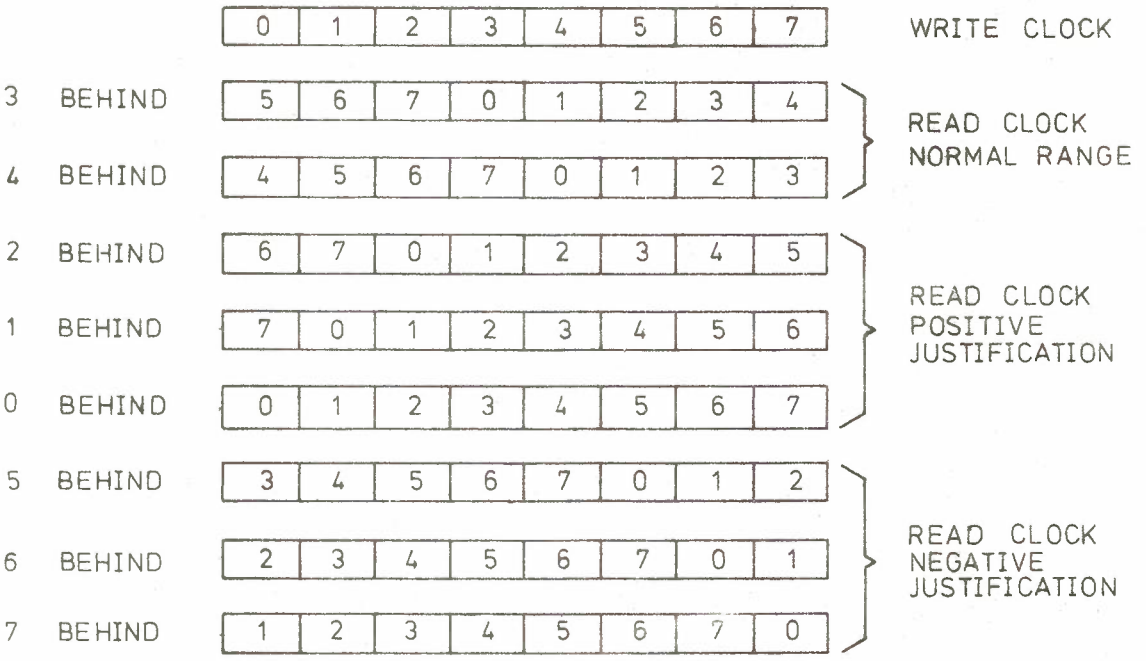


FIG. 4 COMMON CARD TIMING (TRANSMITTER)



OPERATION OF ADDER AND GATING

POSITIVE JUSTIFICATION			NEGATIVE JUSTIFICATION		
2 BEHIND	1 BEHIND	0 BEHIND	5 BEHIND	6 BEHIND	7 BEHIND
0 - 6 = - 6	0 - 7 = -7	0 - 0 = 0	0 - 3 = - 3	0 - 2 = - 2	0 - 1 = - 1
1 - 7 = - 6	1 - 0 = 1	1 - 1 = 0	1 - 4 = - 3	1 - 3 = - 2	1 - 2 = - 1
2 - 0 = 2	2 - 1 = 1	2 - 2 = 0	2 - 5 = - 3	2 - 4 = - 2	2 - 3 = - 1
3 - 1 = 2	3 - 2 = 1	3 - 3 = 0	3 - 6 = - 3	3 - 5 = - 2	3 - 4 = - 1
4 - 2 = 2	4 - 3 = 1	4 - 4 = 0	4 - 7 = - 3	4 - 6 = - 2	4 - 5 = - 1
5 - 3 = 2	5 - 4 = 1	5 - 5 = 0	5 - 0 = 5	5 - 7 = - 2	5 - 6 = - 1
6 - 4 = 2	6 - 5 = 1	6 - 6 = 0	6 - 1 = 5	6 - 0 = 6	6 - 7 = - 1
7 - 5 = 2	7 - 6 = 1	7 - 7 = 0	7 - 2 = 5	7 - 1 = 6	7 - 0 = 7
- 6, 2	- 7, 1	0	- 3, 5	- 2, 6	- 1, 7
- 6 = 1010	- 7 = 1001	0 = 0000	- 3 = 1101	- 2 = 1110	- 1 = 1111
2 = 0010	1 = 0001		5 = 0101	6 = 0110	7 = 0111
DESIGNATE BINARY Nº. xywz			DESIGNATE BINARY Nº. xywz		
$J_+ = x\bar{y}w\bar{z} + \bar{x}\bar{y}wz + x\bar{y}\bar{w}z + \bar{x}\bar{y}\bar{w}z + \bar{x}\bar{y}\bar{w}\bar{z}$ $= \bar{y}\bar{w}z + \bar{x}\bar{y}\bar{w} + \bar{y}w\bar{z}$			$J_- = xy\bar{w}z + \bar{x}y\bar{w}z + xyw\bar{z} + \bar{x}ywz + xywz + \bar{x}ywz$ $= yz + yw$		

FIG. 5 OPERATION OF JUSTIFICATION DETECTION

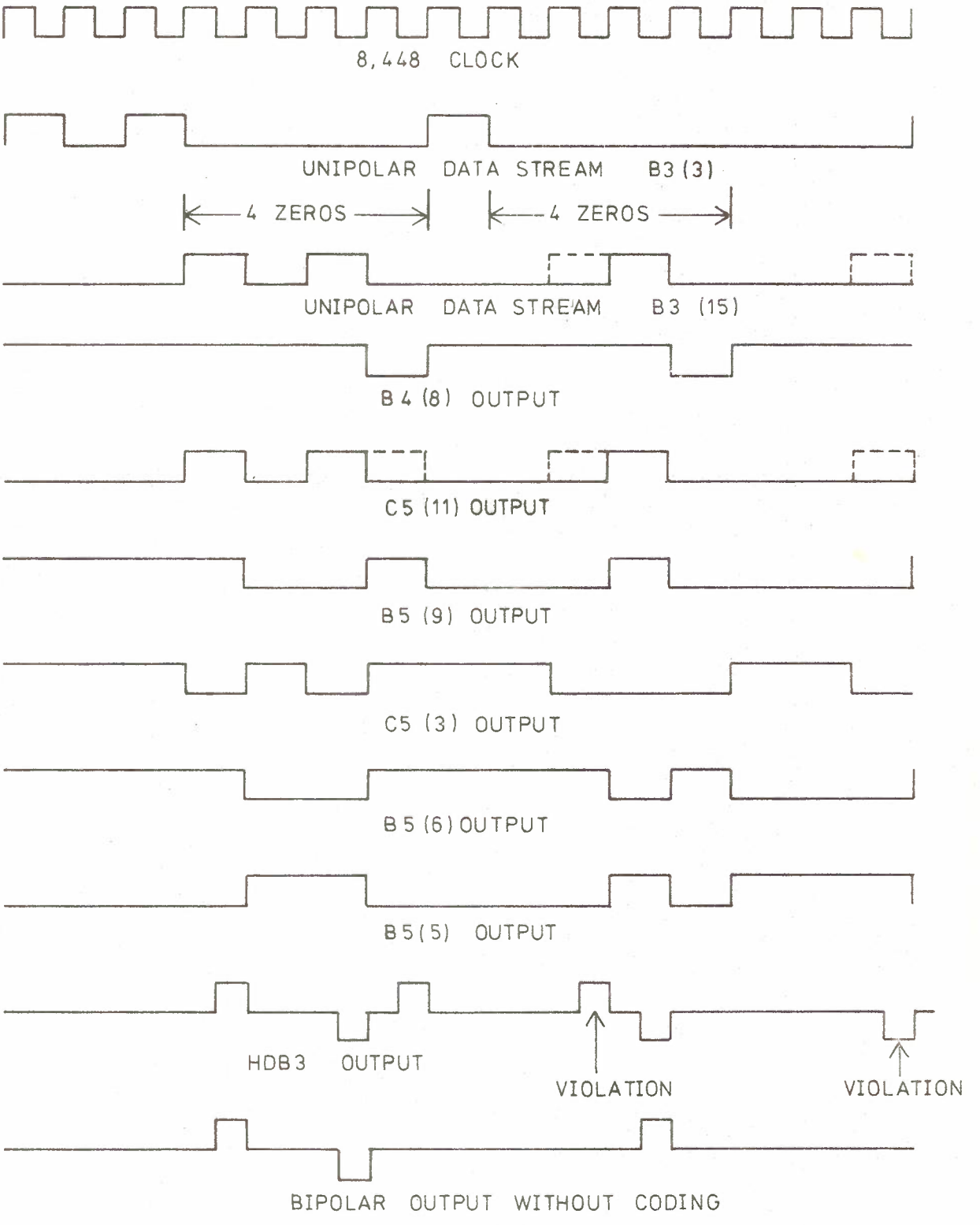


FIG. 6 TYPICAL HDB3 CODER WAVEFORMS

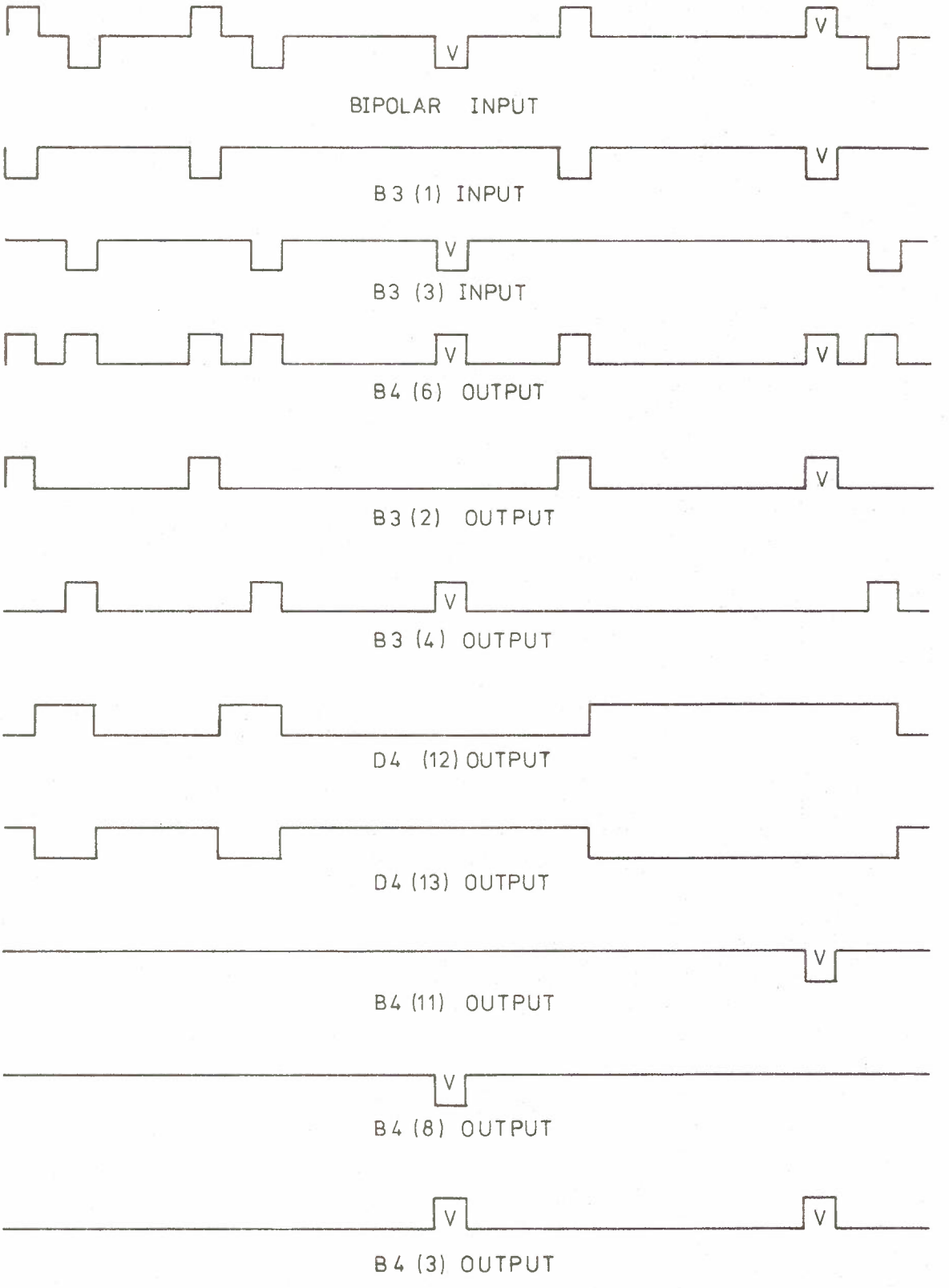


FIG. 7 TYPICAL BIPOLAR VIOLATION DETECTION WAVEFORMS

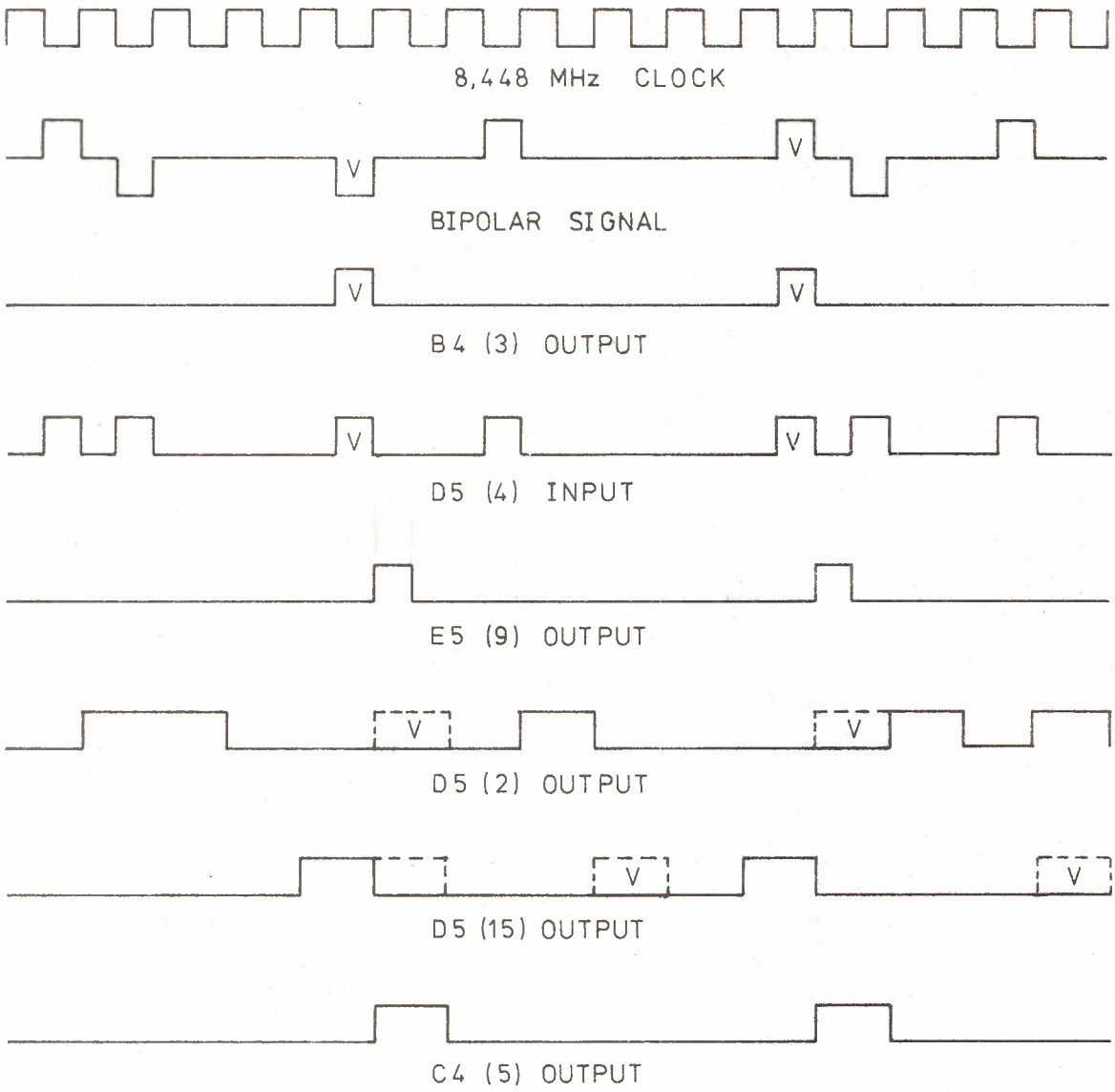


FIG. 8 TYPICAL HDB3 DECODER WAVEFORMS

6890

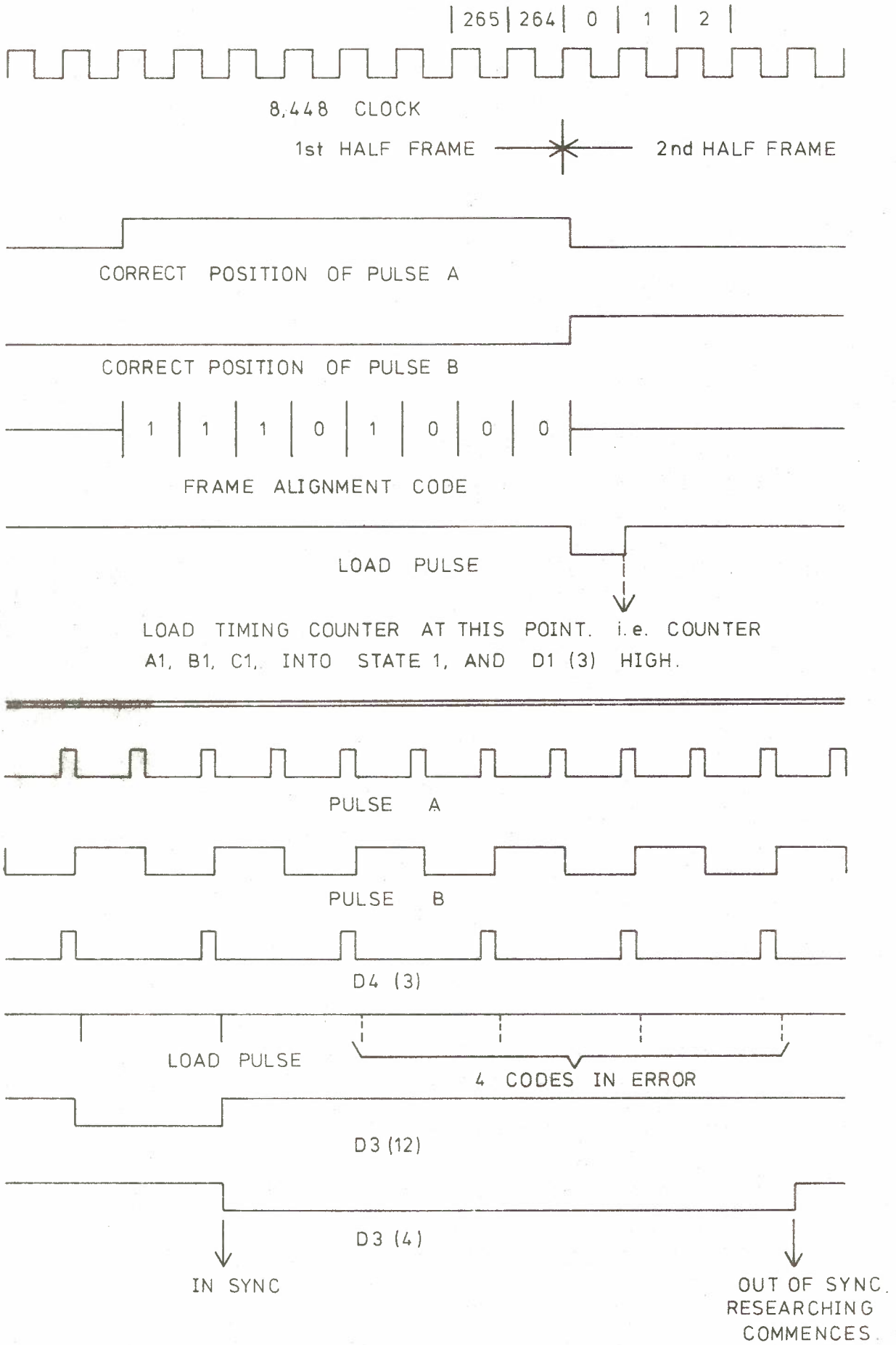
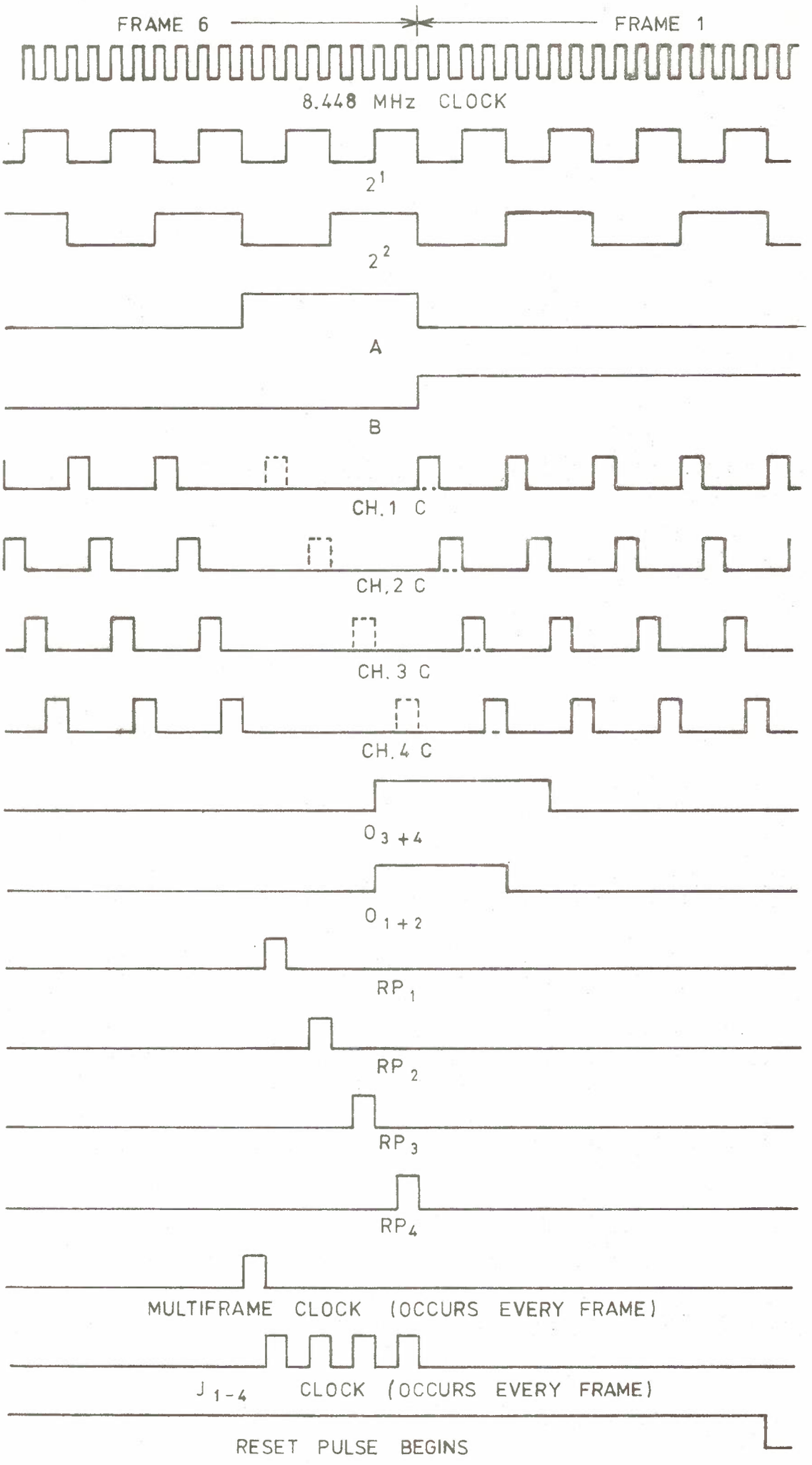


FIG. 9 OPERATION OF FRAME SYNCHRONIZATION



6890

FIG. 10. COMMON CARD TIMING (RECEIVER)

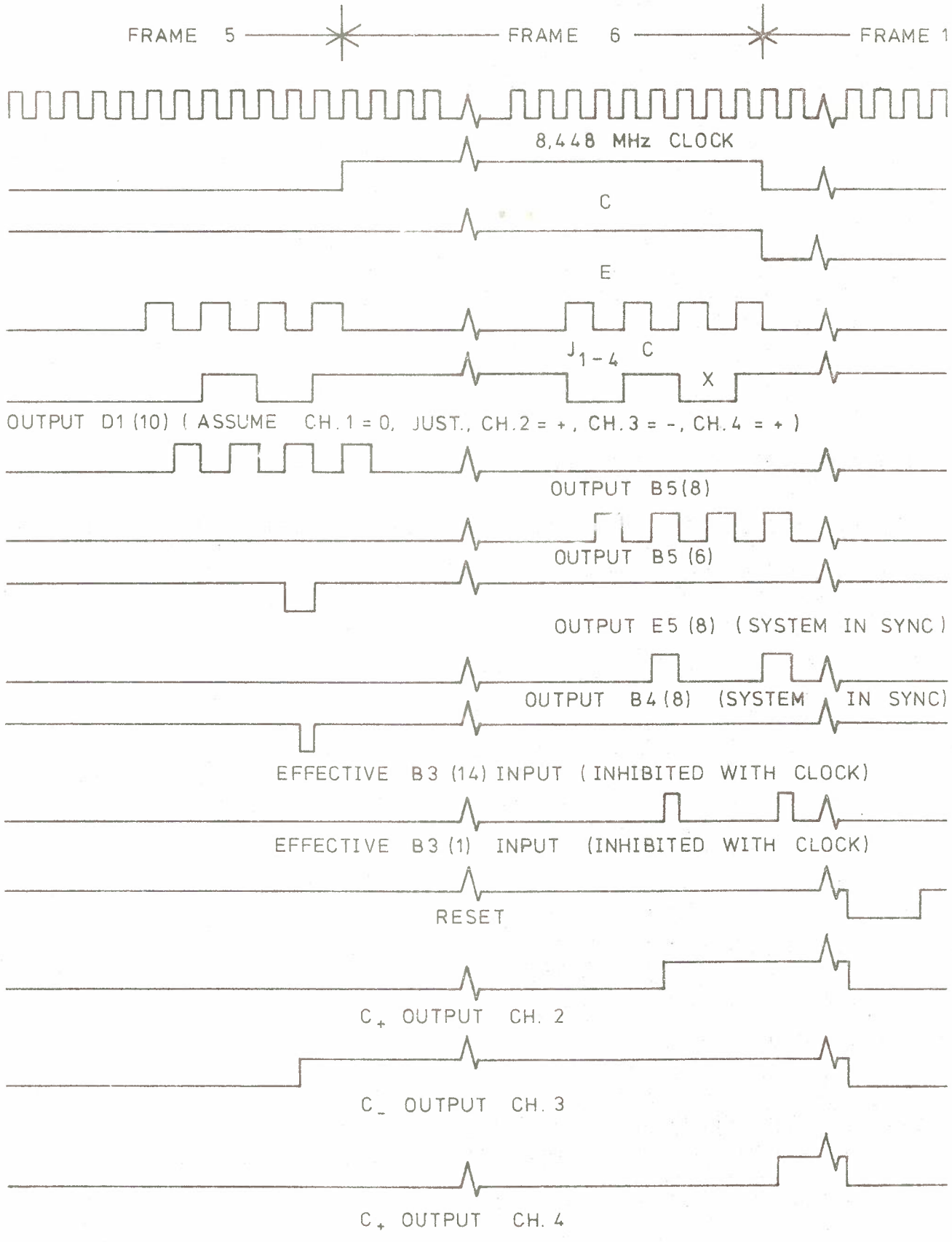
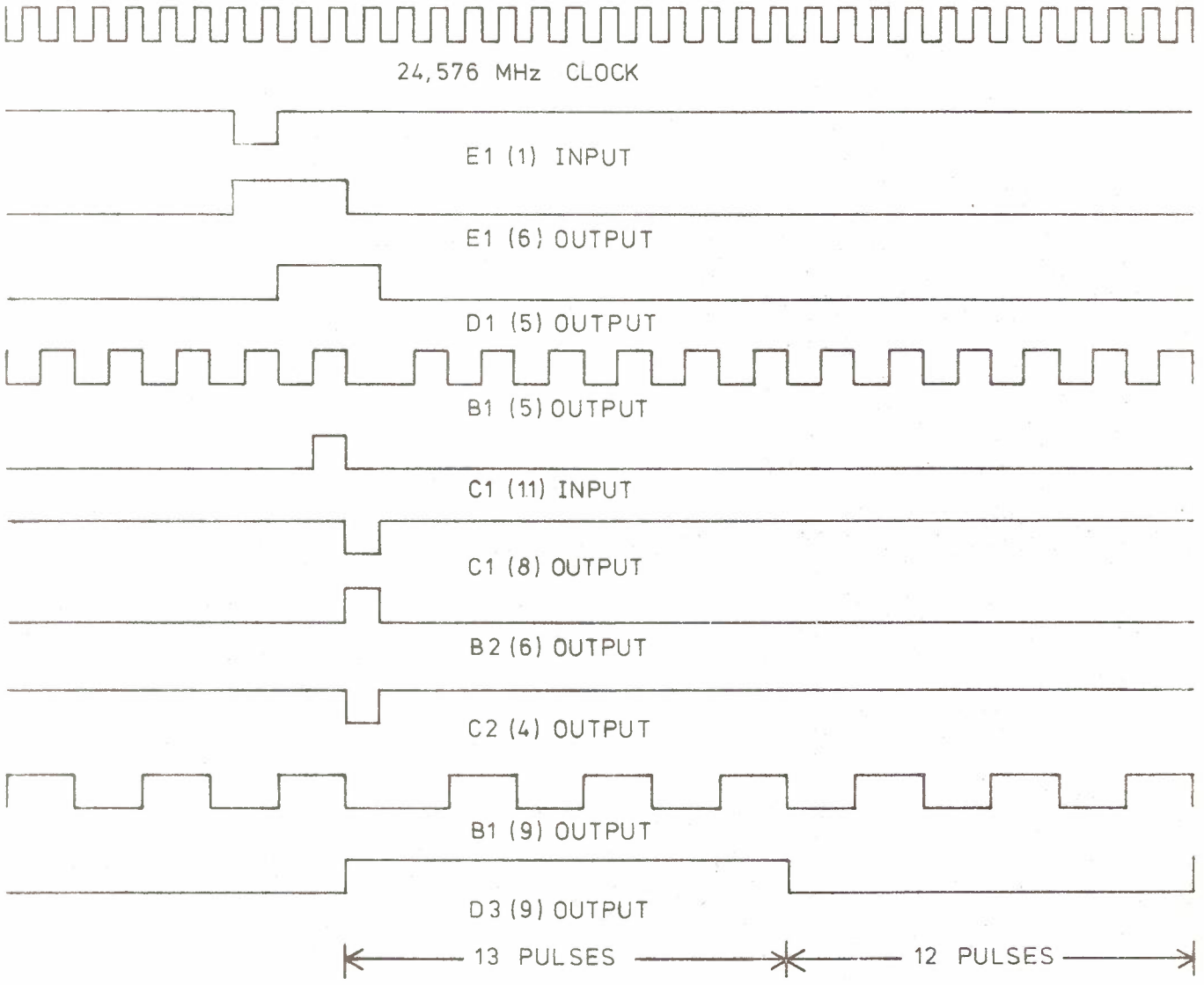
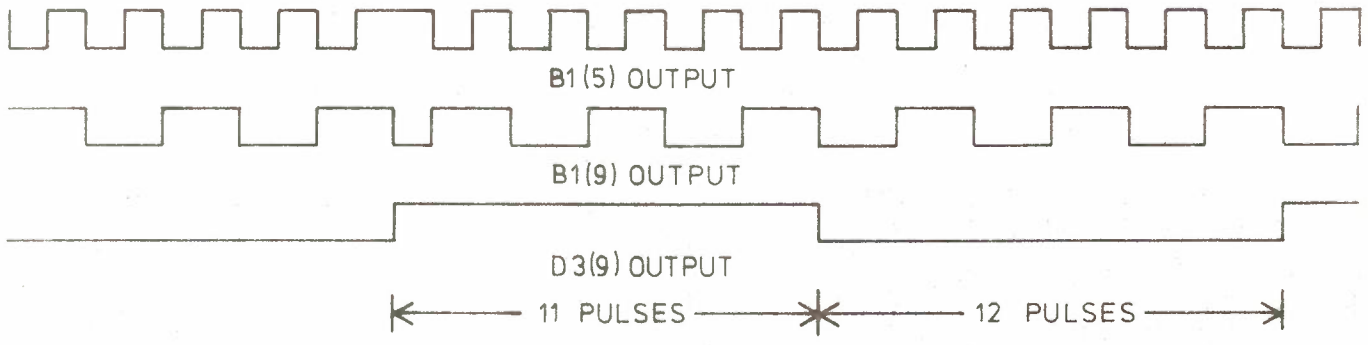


FIG. 11 TYPICAL JUSTIFICATION CODE DETECTION WAVEFORMS



TYPICAL WAVEFORMS FOR POSITIVE JUSTIFICATION



TYPICAL WAVEFORMS FOR NEGATIVE JUSTIFICATION

FIG. 12 OPERATION OF SMOOTHER DIVIDER

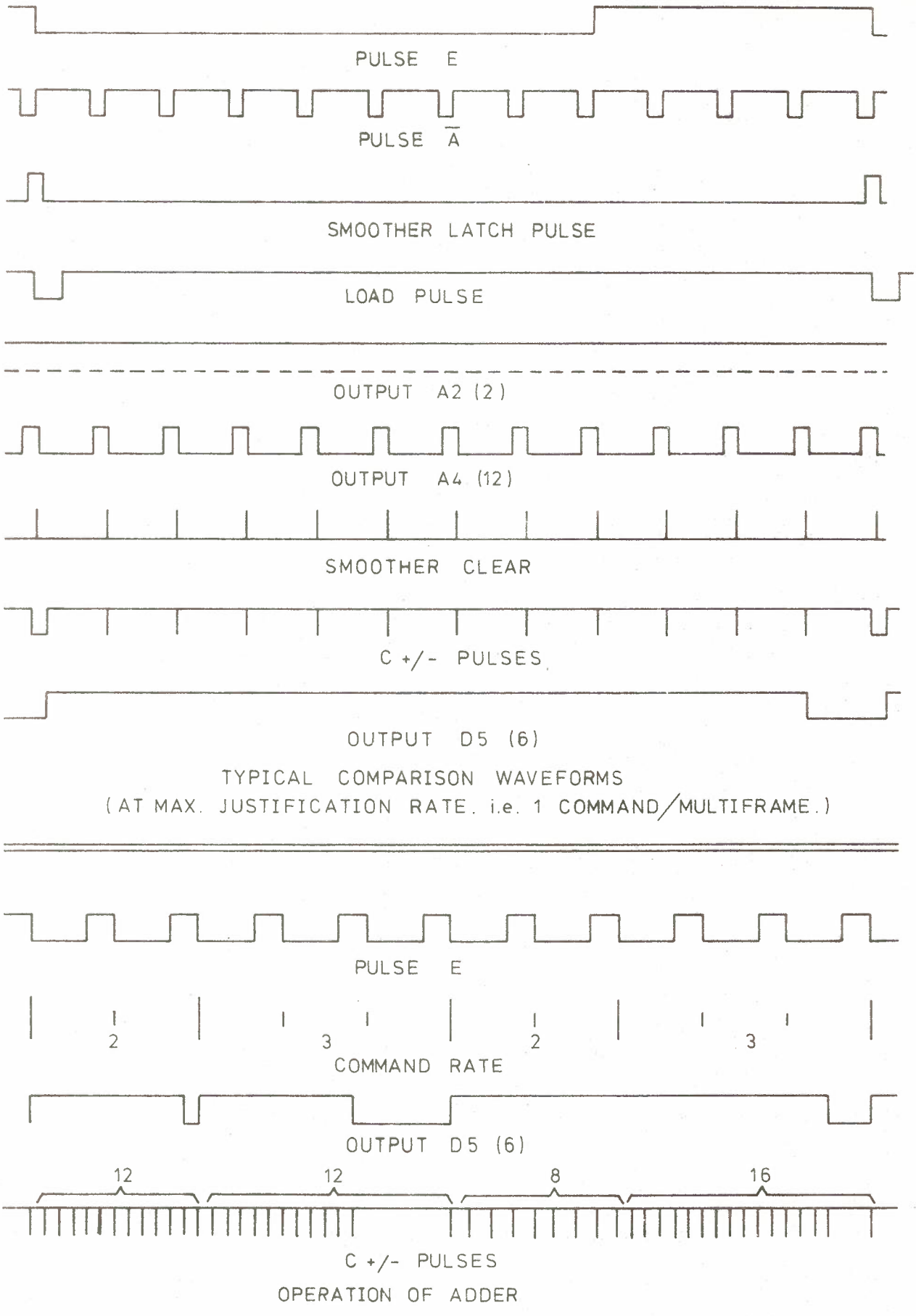


FIG. 13 TYPICAL SMOOTHER CARD WAVEFORMS

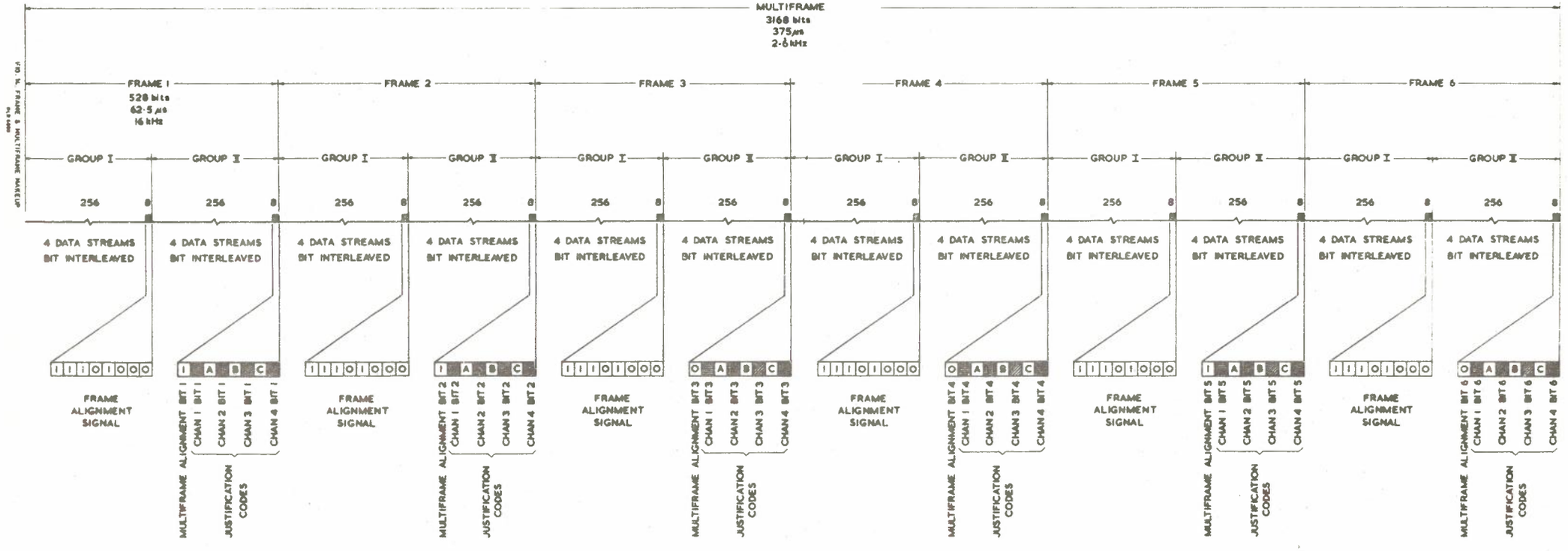
JUSTIFICATION CODES

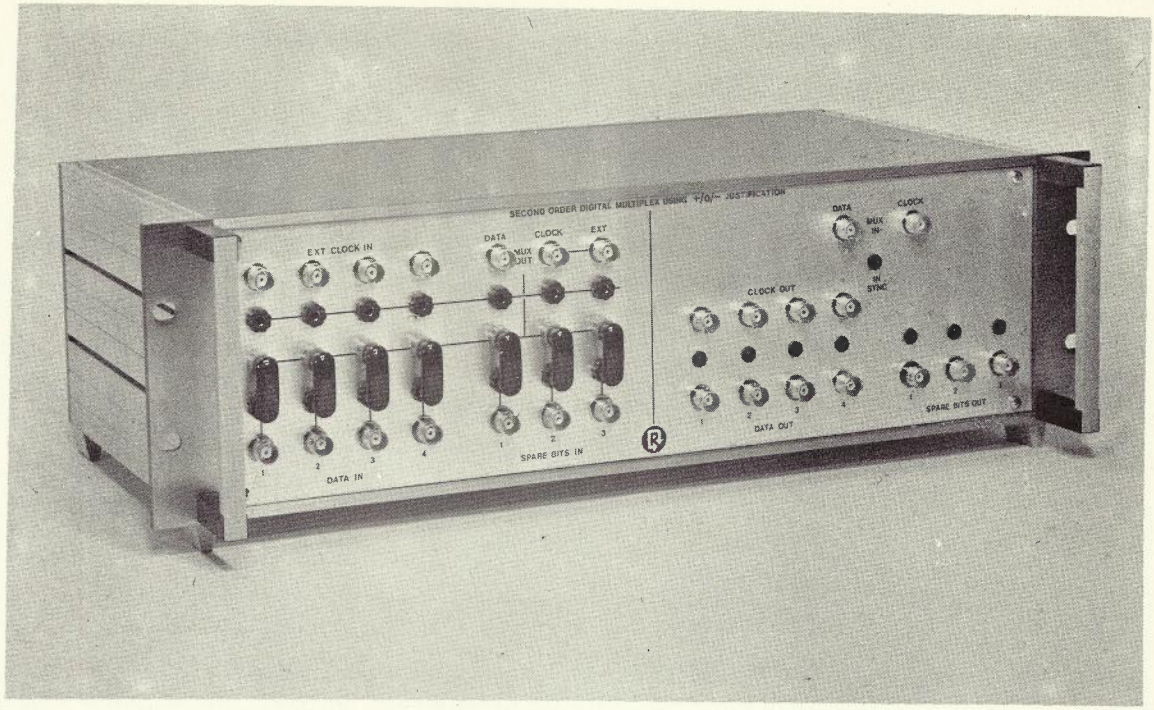
00100 - NO JUSTIFICATION
00111 - POSITIVE JUSTIFICATION
11000X - NEGATIVE JUSTIFICATION
X = ERASED BIT

A = SPARE BIT 1
B = SPARE BIT 2
C = SPARE BIT 3

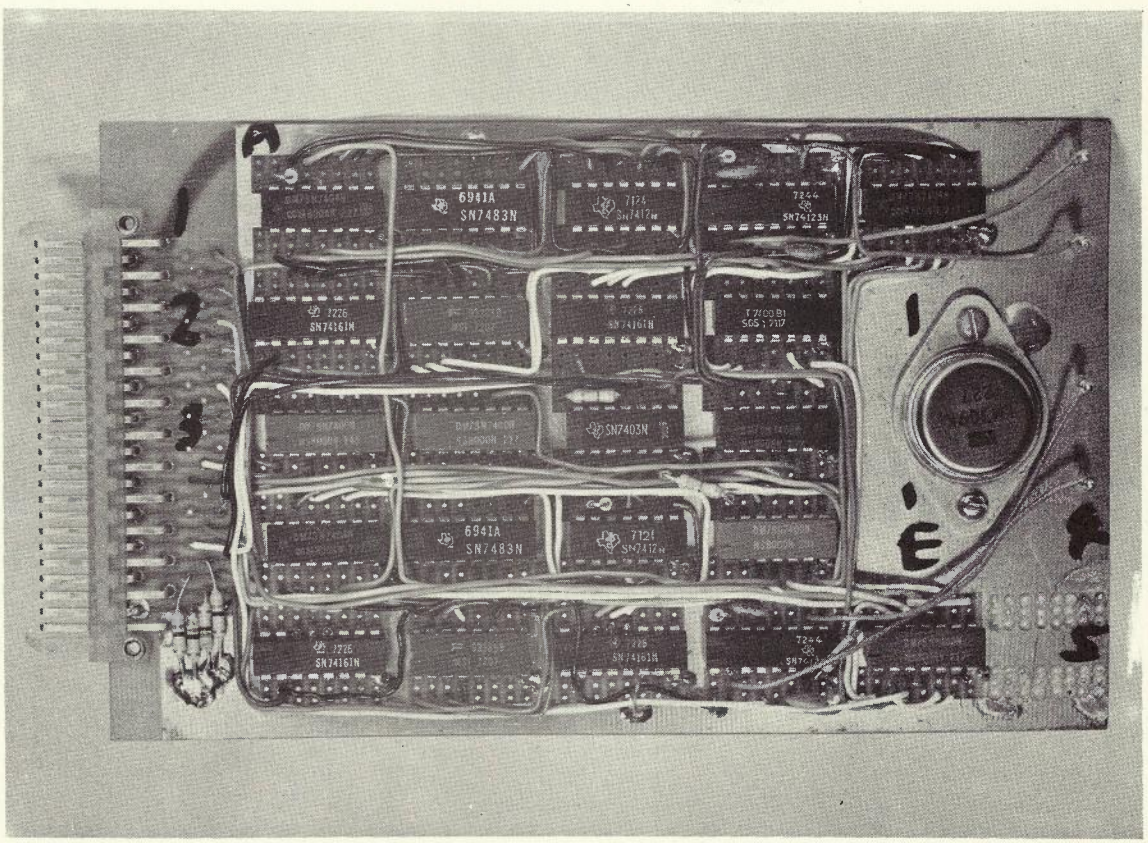
ALIGNMENT CODES

110010 - MULTIFRAME ALIGNMENT CODE
1101000 - FRAME ALIGNMENT CODE





Front View of Multiplex



Typical Card Layout

Fig. 15