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REPORT 7114

LABORATORY TESTS ON A COMMERCIALLY AVAILABLE DATA MULTIPLEX

BY R. COXHILL

Telecom Australia

Telecom Australia

Research Laboratories

770 Blackburn Road, Clayton, Victoria, Australia 3168

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SUMMARY

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BY R.B. COXHILL

At the present time Telecom Australia is conducting studies associated with the introduction of time division multiplexing for Datel services into the Australian network. As part of these studies the Engineering Department has purchased two sets of commercially available synchronous data multiplexes for evaluation. The Research Department has conducted a series of tests on the multiplex equipment and the results are given in the report.

The synchronous data multiplex tested is a general purpose, synchronous time-division multiplex. Up to 32 low speed synchronous data channels can be multiplexed onto a single high speed data stream. Internal programming can cater for a high speed bit rate of up to 1544 kbit/s, with a variety of low speed channel bit rates. The units are normally supplied preprogrammed to the customers high and low speed bit rate and interface specifications. However, programming can be changed by the customer although it is rather complex.

In some system configurations where the low speed channel bit rates are not sub-multiples of the high speed bit rate, the multiplex will produce burst isochronous low speed clocks which are not suitable for most systems where low speed channels interface with synchronous low speed modems. This would be a problem with a high speed bit rate of 64 kbit/s and the standard low speed rates of 1.2, 2.4, 4.8, and 9.6 kbit/s but not with a high speed bit rate of 48 kbit/s.

The results of tests for channel delay indicate that the delay is high, in the order of 10-20 bits, for a bit interleaved multiplex. In most other electrical tests the multiplex performed satisfactorily.

Mechanically, the multiplex has some shortcomings, and the interface is not compatible with ISO recommendations.

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Ambar Banerjee
for Director, Research
31-3-1978

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LABORATORY TESTS ON A COMMERCIALLY AVAILABLE DATA MULTIPLEX

1. INTRODUCTION

Two sets of Timeplex SMC-210 synchronous data multiplexes have been purchased by the Engineering Department as part of a program to study time division multiplexes and their use in the Australian network.

The Research Department was asked to conduct a series of tests on these multiplexes, and two multiplexes were tested.

Throughout this report a "multiplex" is defined as both a transmitter (multiplexer) and a receiver (demultiplexer). "Low speed" signals refer to the data to be multiplexed or having been demultiplexed, or the clock(s) associated with that data. "High speed" signals refer to the multiplexed line data stream, or the clock(s) associated with that data.

2. GENERAL EQUIPMENT DESCRIPTION

The Timeplex SMC-210 synchronous data multiplex is a general purpose, synchronous time-division multiplex. Up to 32 low speed synchronous data channels can be multiplexed onto a single high speed data stream. Internal programming can cater for a high speed bit rate of up to at least 1544 kbit/s, with a variety of low speed channel bit rates. Internal programming is rather complex and is normally not undertaken by the customer. The units are normally supplied pre-programmed to customer specifications.

The multiplexes supplied to the Engineering Department were programmed for a high speed bit rate of 64 kbit/s, with one low speed channel at 800 bit/s, four at 2.4 kbit/s and four at 4.8 kbit/s.

The method employed in the multiplex to produce the necessary low speed clocks is by a division of the high speed clock. When the low speed rates are not sub-multiples of the high speed clock, the low speed clocks are produced by dividing the high speed clock and deleting clock pulses in the divided clock to obtain a low speed clock which has on average the required rate. This produces gaps in the low speed clock pulse train. Such clock signals are often called burst isochronous clock signals. The standard low speed rates of 1.2, 2.4, 4.8 and 9.6 kbit/s etc., are not sub-multiples of 64 kbit/s. Thus, when using these speeds, burst isochronous low speed clocks would be produced. Phaselock loop techniques in producing the low speed clocks would be a way of producing regular clocks in all cases, but such methods are not used.

Most synchronous modems will not operate correctly when fed with a burst isochronous clock signal.

However, most terminals will operate with a burst isochronous clock signal. Therefore, a burst isochronous clock signal can be used when the multiplex and terminals are located so close that low speed modems are not required. However, if low speed modems are required, burst isochronous clock signals can normally not be used.

With this in mind it was arranged for two multiplexes to be reprogrammed. The high speed data rate was reprogrammed to 48 kbit/s, with two low speed channels at 600 bit/s, two at 1.2 kbit/s, two at 2.4 kbit/s, two at 4.8 kbit/s and one at 9.6 kbit/s. With the exception of one of the 600 bit/s channels (bits stolen for synchronizing, see para 5.1) all low speed output clocks are regular for the reprogrammed multiplexes.

No special channels are provided on the multiplex for transfer of control information as is common for asynchronous data multiplexes (Ref. 1) or for synchronous CCITT X-50 type multiplexes (which use envelopes). However, if required, one of the lower speed channels in the system could be used for this purpose.

3. CLOCKING ARRANGEMENTS AND ELASTIC MEMORY POSITIONS IN SYNCHRONOUS MULTIPLEXES

Fig. 1 shows a simplified drawing of the clocking arrangements and elastic memory (sometimes called buffer, elastic buffer, or termed "phasor" in Timeplex literature) positions in most synchronous multiplexes. Elastic memories are usually arranged so that they will be reset to their optimum operating position if they should overflow or become empty.

The function of each elastic memory is as follows:

(i) Low-speed Send Elastic Memory

The main use of this elastic memory is to allow for phase variations due to transmission delay variations and jitter that may occur on the low speed received data.

The elastic memory is also useful for half duplex operation where low speed data coming into the multiplexer is under control of an independant modem clock. Because the bit rate of the incoming data and the multiplexer clock are not synchronised, "slip" (see para 5.5) will occur at periodic intervals. The use of an elastic memory will increase the interval between slips giving longer periods of error free operation than if an elastic memory had not been used.

(ii) Low-speed Receive Elastic Memory

The low speed receive elastic memory is provided on the SMC-210's because in some multiplex configurations the low speed clocks may be burst isochronous clocks (see para 2), and some buffering is required between when data is demultiplexed and when data is made available at the low speed output. In configurations where regular clocks are generated, the low-speed receive elastic memory may not be required, dependant on the frame structure used.

In addition, when it is necessary to externally clock data out of the low speed receive elastic memory using an independant clock, the elastic memory could be used to increase the interval between slips similarly as for the low speed send elastic memory. However, the Timeplex SMC-210's do not provide a means of externally clocking data out of the low speed receive elastic memory.

(iii) High Speed Receive Elastic Memory

This elastic memory is provided to allow for any transmission delay variations or phase jitter in the high-speed receive data stream.

4. SELF TEST AND FAULT LOCATION FACILITIES

The self test and fault location facilities provided on the multiplex appear to be adequate in that most sections of the multiplex can be tested, and most of the important data signals can be monitored. The facilities are listed here:

(i) Low and high-speed data activity indication.

(ii) Low and high-speed modem carrier state indication.

(iii) Low and high-speed phasor (elastic memory) overflow indication.

(iv) Manual resetting of high speed phasor.

(v) Local and remote out-of-synchronization indication.

(vi) Indication of the number of times that the local demultiplex has lost synchronization or an incorrect synchronizing bit has been received (max count seven).

(vii) Manual insertion of errors onto the synchronizing bits sent to line to test facilities (v) and (vi) at local (with high speed busback) or remote demultiplexer.

(viii) Low or high-speed busback (loopback).

(ix) Injection of test characters to low speed send channel with error monitoring and manual error injection into test character.

5. MEASUREMENTS AND RESULTS

5.1 Frame Structure

Frame structure is basically dependent on internal programming. Bit interleaving is used to multiplex low speed channels and mixing of different channel rates is performed by servicing higher

rates more often than slower rates. Synchronization is achieved by stealing bits from one of the slowest speed data channels and replacing them with a synchronizing pattern of 1 0 0 0. The position of bits stolen for synchronization is variable, subject to internal programming. Fig. 2 shows the frame structure of the units tested by the Research Department. Note that the frame duration is 113.3 ms.

5.2 Loss and Recovery of Frame Synchronisation

Fig. 3 shows the test setup. Waveforms and times associated with this test are shown in Fig. 4 and Fig. 5.

The multiplex is equipped with a monitoring point which provides information as to whether the demultiplexer is in or out of synchronization. The waveform available at this point is referred in the text and the drawings as the "IN/OUT synchronization pulse".

Clock and/or data fed to the demultiplexer were interrupted for a period of approximately 2 seconds or more. The break time was varied slightly to obtain maximum and minimum times to go in and out of synchronization. Only one input channel was active during the test. When all channels are active, the frame recovery time may be higher than measured due to a higher chance of frame word simulation.

5.2.1 Clock and Data Interrupted. The average time to lose synchronization corresponded to 3.5 frame periods. As shown in Fig. 4 the demultiplexer registered "in synchronization" for approximately 1 frame period whilst the line break was still in progress. It was also found that if the line break was of sufficient duration, the demultiplexer would register "in synchronization" at periodic intervals of approximately 1.4 seconds (or approximately 12 frame periods).

The time to regain synchronization varied from a very short period to approximately 1.3 seconds, and appeared to be controlled by the position of the termination of the break pulse in relation to the state of the In/Out sync. pulse. Referring to Fig. 4 if the break pulse terminated at point "A", time to regain synchronization was very low. However, if the break pulse terminated at point "B", time to regain synchronization could be up to 1.3 seconds, (about 11.5 frame periods).

It should be noted that interrupting both clock and data is a severe test as many modems will continue to supply a clock signal (free running) during a line break, and thus interruption of both clock and data is unlikely to occur.

5.2.2 Data Only Interrupted. The average time to lose synchronization corresponded to 1.5 frame periods (high speed line fixed to "high" during interrupt) or 5.5 frame periods (high speed line fixed to "low" during interrupt). The time to regain synchronization corresponded to an average of 0.5 frame periods in both cases.

As noted in section 5.2.1, during a line break condition, many modems continue to supply a clock signal, whereas the data will normally be in a steady state. Therefore the case considered in this section will be typical in a line break (interruptions) situation.

5.3 Error Sensitivity of Frame Synchronization. Fig. 3 shows the test setup. Errors were inserted onto the high speed data stream with an error insertor. The operation of the error insertor is described in Ref. 1. Basically the high speed signal is subjected to white noise causing both single and burst errors. The error rate inserted onto the high speed data stream was increased until the first occurrence of the out of synchronization alarm, within an observing time of a few seconds.

Results showed that the high speed data error rate had to be in the vicinity of 1.5 in 10^1 before the out of synchronization alarm was registered within a few seconds. This insensitivity of the frame synchronization against bit erros will be mainly due to the low rate of the synchronization information (one sync. bit per 28.3 ms or a rate of 35 bit/s). This indicates that two successive synchronization bits must be in error before frame synchronization is assumed to be lost. With this assumption and an error rate of 1.5 in 10^1, it can be calculated that frame synchronization will be lost, on average, every 6 seconds after synchronization is established.

In a practical situation, the error rate will normally not be much lower than 1 in 10^4 which will mean that the average time between frame synchronization loss due to errors is about 33 days or better (if our interpretation of the frame strategy used is correct).

5.4 Ratio of High Speed Error Rate/Low Speed Error Rate.

Fig. 3 shows the test setup.

The high speed error rate was set to between 1 in 10^4 and 1 in 10^5. High and low speed errors were counted over a fixed period and error rates calculated. Ideal measuring conditions should give a high/low speed error rate ratio of 1:1. The results of measurements taken in this test showed that the ratio of high/low speed error rate was very close to the ideal of 1:1 (that is the high and low speed error rates are close to equal).

In conclusion, this test indicates that no unnecessary errors are introduced by the multiplex.

5.5 Capacity of Demultiplexer Elastic Memory.

High speed data fed into the demultiplexer is fed into an elastic memory by the high speed modem receive clock, and read out of the elastic memory by the high speed modem send clock (see also para 3). According to the handbook the elastic memory has a capacity of ±16 bits, and is automatically reset to its midpoint if it overflows or empties.

To test the elastic memory capacity the test setup shown in Fig. 6 was devised. Basically the measurement technique is to compute the number of bits between high speed send and receive clock signals over one "in synchronization" period. Slip (the loss or repetition of bits) will occur if there is a frequency difference between the high speed send and receive clock. Due to slip the frame

synchronization will be lost as some frames do not contain the correct number of bits. Normally the high speed send and receive clocks are in synchronism and temporary phase variations are absorbed in the demultiplexer elastic memory. In this test a small frequency difference (about 1 Hz) was forced between send and receive clock to measure the elastic memory's capacity. A 64 bit elastic memory was added between the high speed data send and receive connection points to provide buffering for the high speed data stream, as the high speed data had to be retimed for proper operation.

Briefly the method is as follows:

Events counter 1 counts high speed send clock pulses. Events counter 2 counts high speed receive clock pulses. Both counters commence counting when the demultiplexer comes in synchronization, and stop counting when the demultiplexer loses synchronization. It is assumed that demultiplexer elastic memory has filled or emptied when the demultiplexer loses synchronization. Care was taken to ensure that loss of demultiplexer synchronization was not due to the added 64 bit elastic memory overflowing or emptying. Logic is arranged so that the counters can only count during one "in synchronization" period. Synthesiser 1 is set at 48 kHz. Two separate tests were performed with synthesiser 2 then get 1 Hz faster and 1 Hz slower than synthesiser 1. The difference in readings between the two counters at the close of counting was taken to be the demultiplexer elastic memory capacity. All tests were repeated a number of times and gave consistent results.

Results:

- capacity (memory emptying, receive clock faster) - 15 bits.

+ capacity (memory filling, receive clock slower) - 14 bits.

In this test, essestially the difference in bit count over a period is measured.

The accuracy of each counter is ±1 count, thus the total accuracy is ±2 counts or ±2 bits. As the results obtained in each test were consistent, it is likely that the actual accuracy of the measured buffer capacity is better than ±2 bits. More accurate results could be obtained by frequency multiplying the send and receive clocks that are fed to the event counters by a common factor.

In conclusion, it was measured that phase variations of up to -15 or +14 bits (29 bits peak to peak) could be absorbed in the high speed elastic memory before slip in the high speed bit stream occured.

5.6 Capacity of Low Speed Elastic Memories

Elastic memories are used in every low speed send and receive data channel. According to the handbook each elastic memory can absorb ±4 bits of data, and is automatically reset to its midpoint if it overflows or empties.

Fig. 7 shows the test setup, and a simplified drawing of the position of each elastic memory in the multiplex.

The capacity of the low speed receive elastic memory was not tested because no way could be found to test the capacity without internally modifying circuitry, and this was considered to be too time consuming.

Using the test setup shown in Fig. 7 the capacity of the low speed send elastic memory was tested using the following technique. Synthesiser 2 was set at 48 kHz. Two separate tests were performed with synthesiser 1,1 Hz faster and 1 Hz slower than the actual bit rate of the channel being tested. In each test the error detector would lose synchronization at periodic intervals whenever there was a slip (the elastic memory overflowed or emptied). The error detector was manually resynchronized after each loss of synchronization to enable a successive series of slips to be measured. It is only necessary to resynchronize the error detector before the next loss of synchronization occurs (this happened at a rate 3-4 seconds), in order to avoid any loss of accuracy in the measurement. The number of seconds between successive losses of synchronization is equal to the elastic memory capacity in bits in this case.

Results:

- capacity (memory emptying, synthesiser 1,1 Hz slower). 3 bits.

+ capacity (memory filling, synthesiser 1,1 Hz faster). 4 bits.

Accuracy:

In this test essentially the time between slips is measured. In the case of measuring - capacity, 20 losses of synchronization were recorded over a period of 60 seconds ±1 sec. Thus the accuracy of the measured buffer capacity is close to $\pm \frac{1}{20}$ of a bit.

In conclusion, it was measured thus phase variations of up to -3 or +4 bits (7 bits peak to peak) could be absorbed in the low speed send elastic memory before slip in a channel occurred.

5.7 Channel Delay

Fig. 8 shows the test setup. It was found that the delay through channels varied if the power to the multiplex was interrupted for a short period, or if the low speed input/output connections were interrupted for a short period. Results show the minimum and maximum times that were obtained. The delays appear to be relatively high for a bit interleaved multiplex.

Table 1

Rate (kbit/s)	Channel No.	Delay (ms)	Delay (Bits)
0.6	1 (Sync Channel)	2.5	1.5
0.6	26	15.0 - 21.0	9 - 12
1.2	6	7.0 - 10.0	8 - 12
1.2	12	8.5 - 11.0	10 - 13
2.4	14	5.0 - 6.3	12 - 15
2.4	22	4.7 - 6.4	11 - 15
4.8	3	2.9 - 3.5	14 - 17
4.8	15	3.8 - 4.4	18 - 21
9.6	16	2.6 - 3.1	25 - 30

6. INTERFACES

The multiplex equipment is supplied with electrical interfaces according to customer specifications. The multiplex equipment supplied to the Engineering Department was equipped with low speed electrical interfaces according to CCITT Rec V28, and high speed electrical interfaces according to CCITT Rec V35.

Input and Output connections are made via wire wrap pins. The mechanical interface is not in accordance with International Standards Organisation Recommendations 2110 and 2593 which recommends connectors and pin numbering for use with equipment having electrical interface compatiable with CCITT Recommendations V28 and V35 respectively.

7. MECHANICAL CONSTRUCTION

The mechanical construction would generally be classed as unacceptable. The multiplex is excessively bulky and heavy. Individual cards are difficult to plug in and out. Screws and nuts were found lying in the bottom of the units after they were unpacked. Subsequently in one of the units the screws securing a card socket guide rail were found to be missing. This had the effect of producing intermittent contact between some cards and their sockets. This fault was rectified by the Research Department.

Functionally equivalent cards are provided with different revisions making servicing confusing. Some cards have been modified by soldered wires.

Programming is physically arranged by soldering straps onto dual-in-line "header", and this arrangement was considered satisfactory.

Several electrical faults have occurred during the time the units have been in the Research Department. Both units were sent back once to the Australian agents for repair. The Research Department has not been informed of the cause of the fault in this case. Other faults were a faulty integrated circuit and a faulty transistor in the power supply, which were repaired by the Research Department.

8. DOCUMENTATION

The documentation supplied with the units was for a model SMC 200. The model SMC 210 is considerabley revised and the supplied information for the model SMC 200 was not sufficient to make the units operational. Difficulties were encountered in obtaining all necessary documentation, and some circuit diagrams have yet to be received. The documentation provided is not generally clearly written.

9. CONCLUSIONS

The results of a series of tests on a Timeplex SMC 210 synchronous data multiplex are given in this report. The multiplex performed satisfactorily in most aspects of the electrical tests. The results obtained for channel delay appear to be high for a bit interleaved multiplex. Mechanically the multiplex has some shortcomings in that the units are excessively heavy and bulky and some problems occurred with missing and loose screws. Difficulties occurred with insufficient documentation, and this problem was not entirely solved. Mechanically the interfaces are not compatible with ISO standards 2110 and 2593.

In some system configurations where the low speed channel bit rates are not sub multiplies of the high speed bit rate, the multiplex will produce burst isochronous (irregular) low speed clock pulses which are not suitable for most systems where low speed channels interface with synchronous modems. This would be a problem with a high speed bit rate of 64 kbit/s and the standard low speed rates of 1.2, 2.4, 4.8 and 9.6 kbit/s, but not with a high speed bit rate of 48 kbit/s.

The self test and fault location facilities provided on the multiplex appear to be adequate.

ACKNOWLEDGEMENT

The author wishes to thank Mr. J.A. Bylstra for his assistance in preparation of the report and general guidance with the measurement program.

REFERENCES

1. J.A. Bylstra, "Laboratory Evaluation on Case 670 and Timeplex T-20 Data Multiplex Equipment", R.L. Report No. 7035.

2. CCITT Recommendation V28, Orange Book, Vol. VIII.1, 1976, p.p. 139-143.

3. CCITT Recommendation V.35 Appendix 2, Orange Book, Vol. VIII.1, 1976, p.p. 162-163.

4. ISI Standard No. 2110, Data communication - Data terminal and data communicatcn equipment - Interchange circuits - Assignment of connector pin numbers. Ref. No. ISO 2110 2593 - 1973 (E).

5. ISO Standard No. 2593, Connector pin allocations for use with high-speed data terminal equipment. Ref. No. ISO 2593-1973 (E).

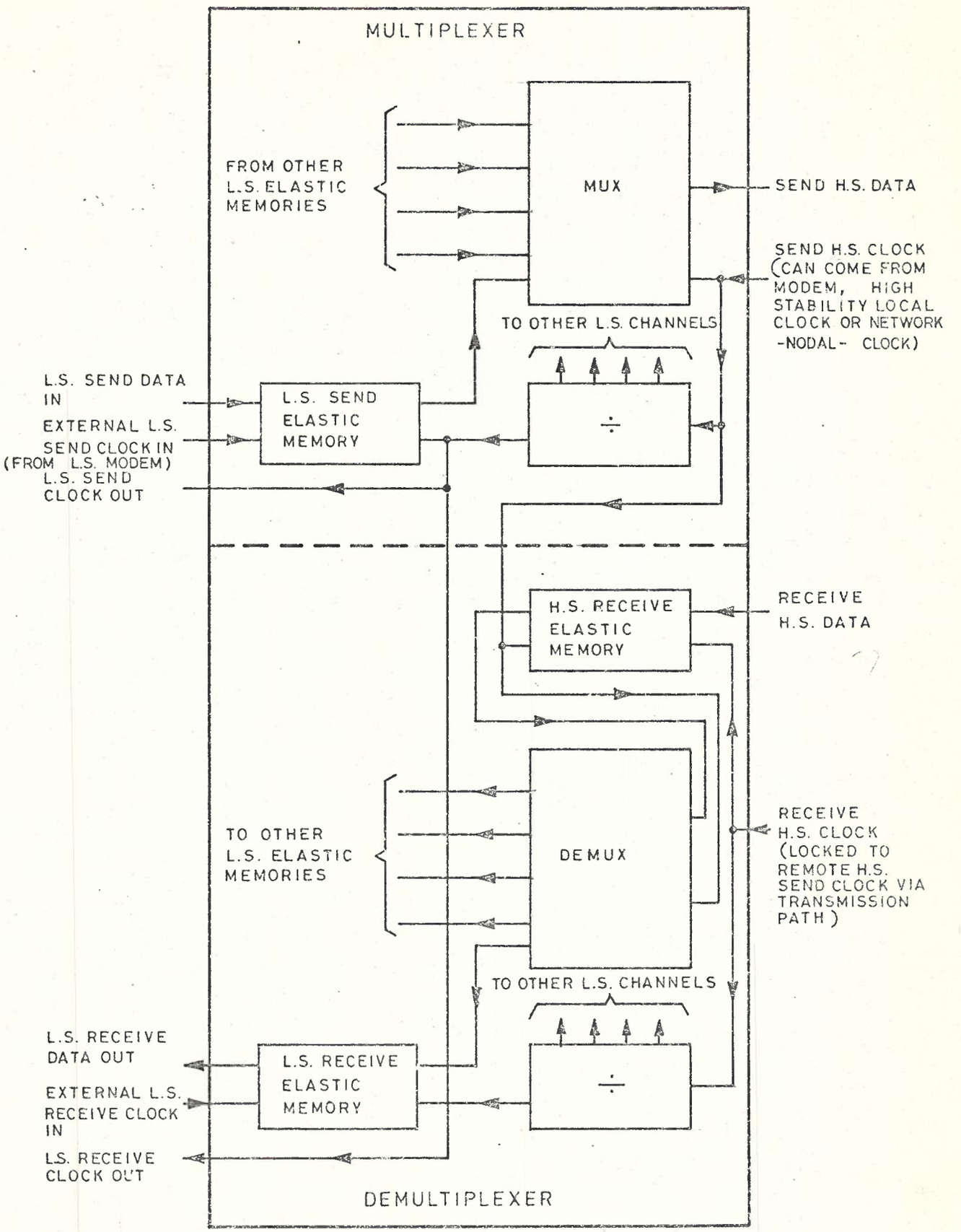


FIG. 1 CLOCKING ARRANGEMENTS AND ELASTIC MEMORY POSITIONS IN SYNCHRONOUS MULTIPLEXES.

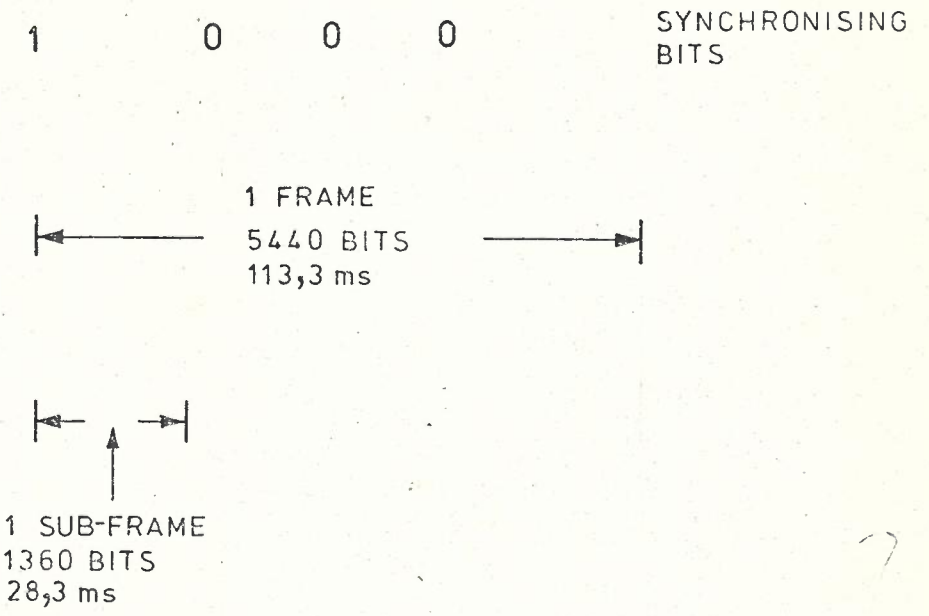


FIG. 2 FRAME STRUCTURE OF SMC 210's TESTED BY RESEARCH DEPARTMENT

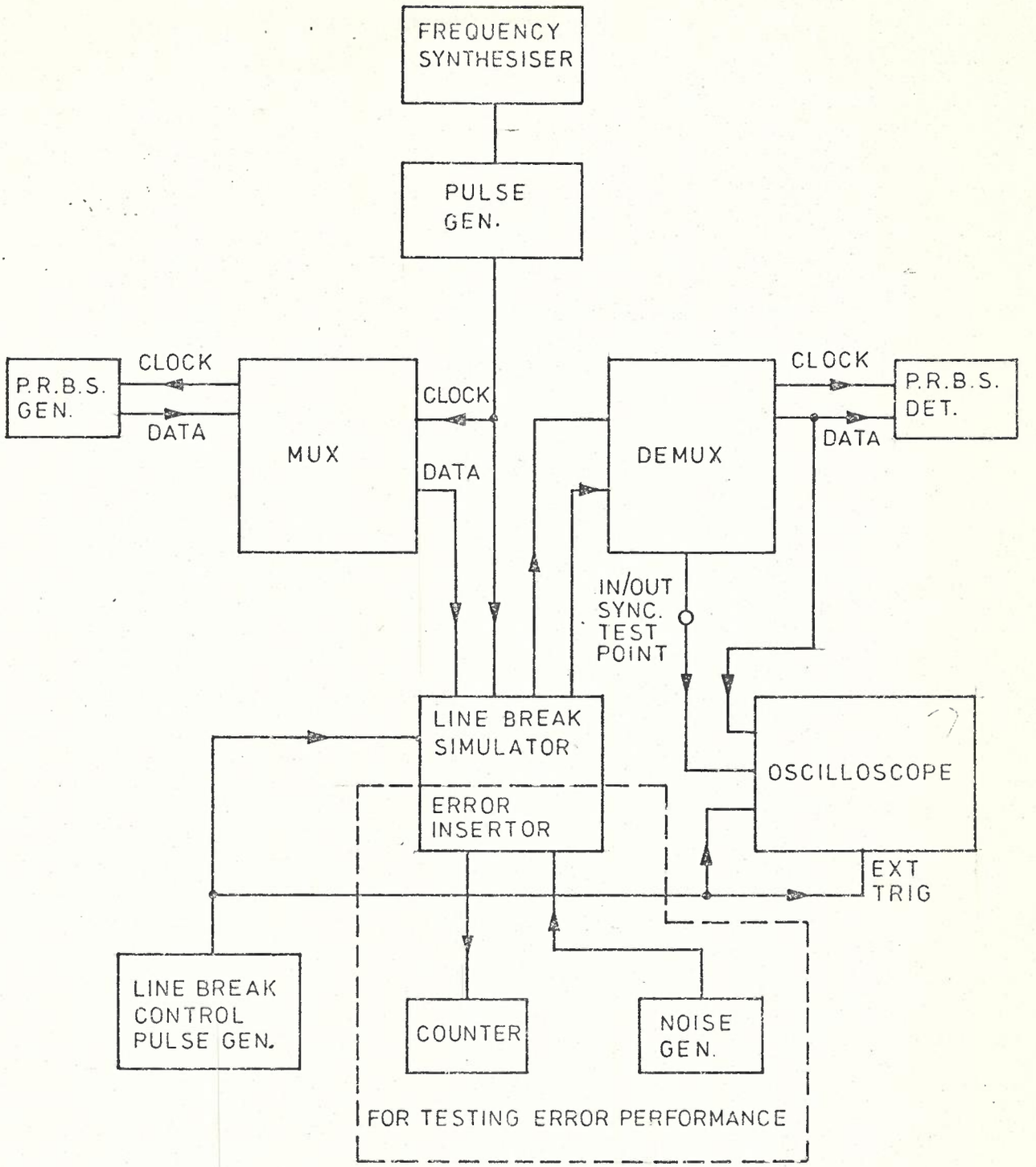
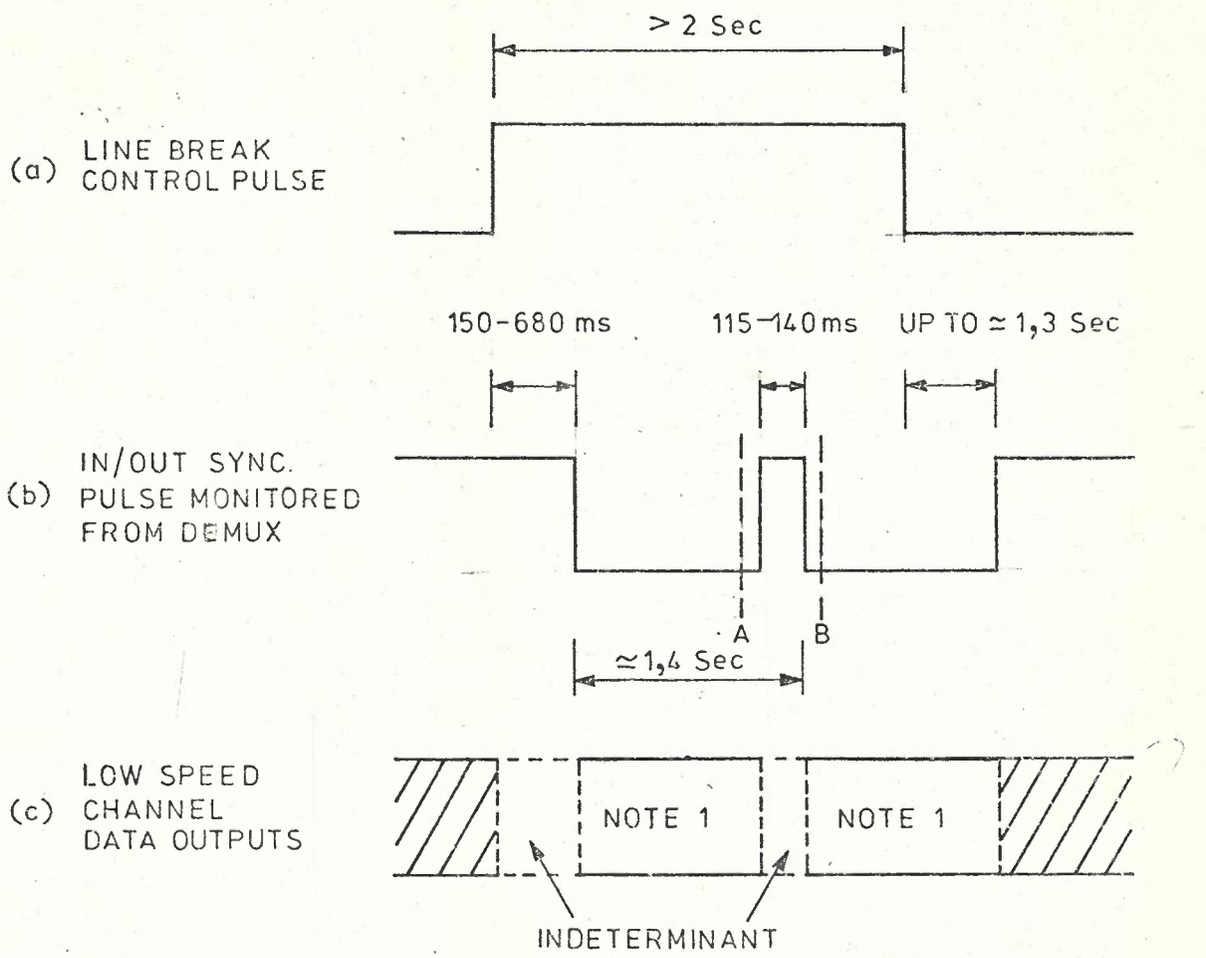


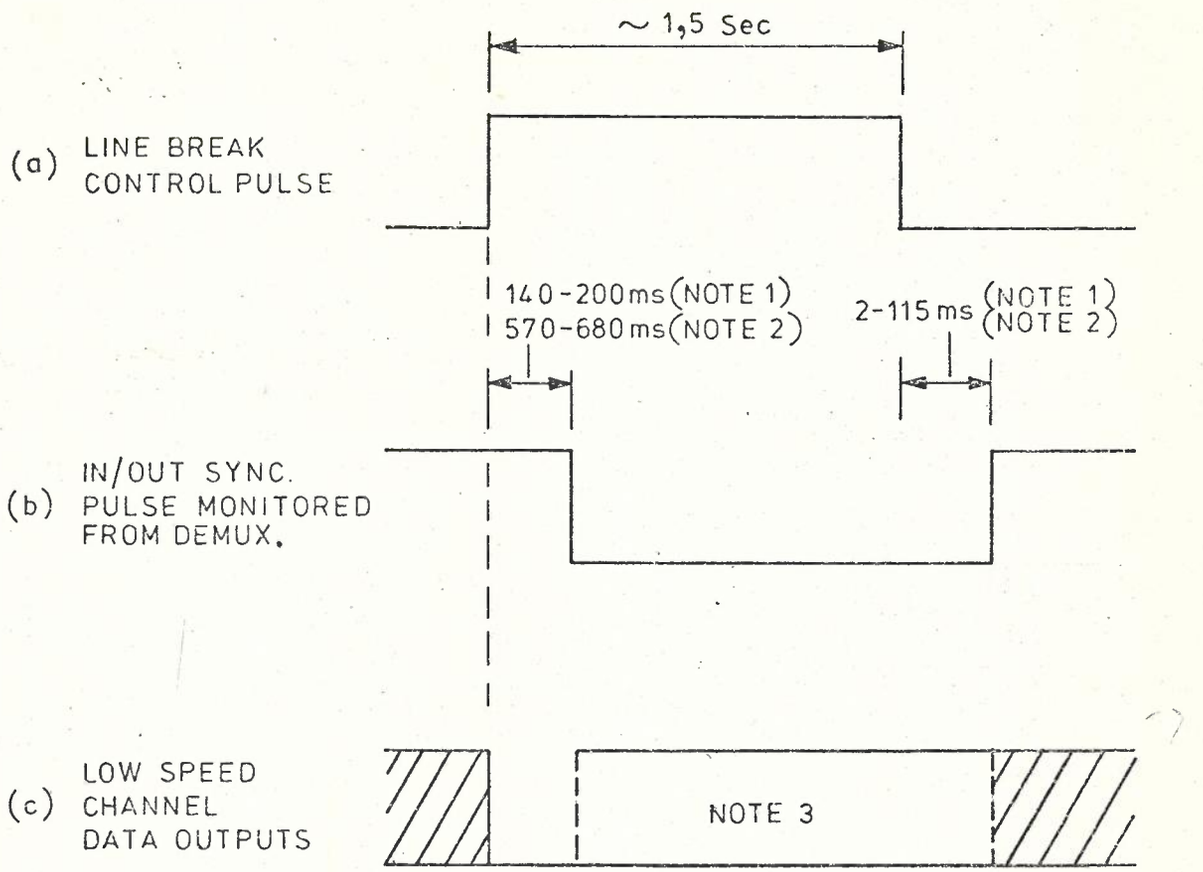
FIG. 3 TEST SETUP FOR MEASUREMENT OF FRAMING AND ERROR PERFORMANCE.



NOTE 1: CAN BE PROGRAMMED TO CLAMP TO "HIGH" OR "LOW" STATE.

NOTE 2: WAVEFORMS ARE THE SAME FOR THE HIGH SPEED LINE FIXED TO "HIGH" OR "LOW" STATE DURING INTERRUPT PERIOD.

FIG. 4. WAVEFORMS ASSOCIATED WITH FRAMING PERFORMANCE (CLOCK AND DATA INTERRUPTED).



NOTE 1: TIME WITH HIGH SPEED LINE FIXED TO "HIGH" STATE DURING INTERRUPT.

NOTE 2: TIME WITH HIGH SPEED LINE FIXED TO "LOW" STATE DURING INTERRUPT.

NOTE 3: CAN BE PROGRAMMED TO CLAMP TO "HIGH" OR "LOW" STATE.

FIG.5 WAVEFORMS ASSOCIATED WITH FRAMING PERFORMANCE. (DATA ONLY INTERRUPTED.)

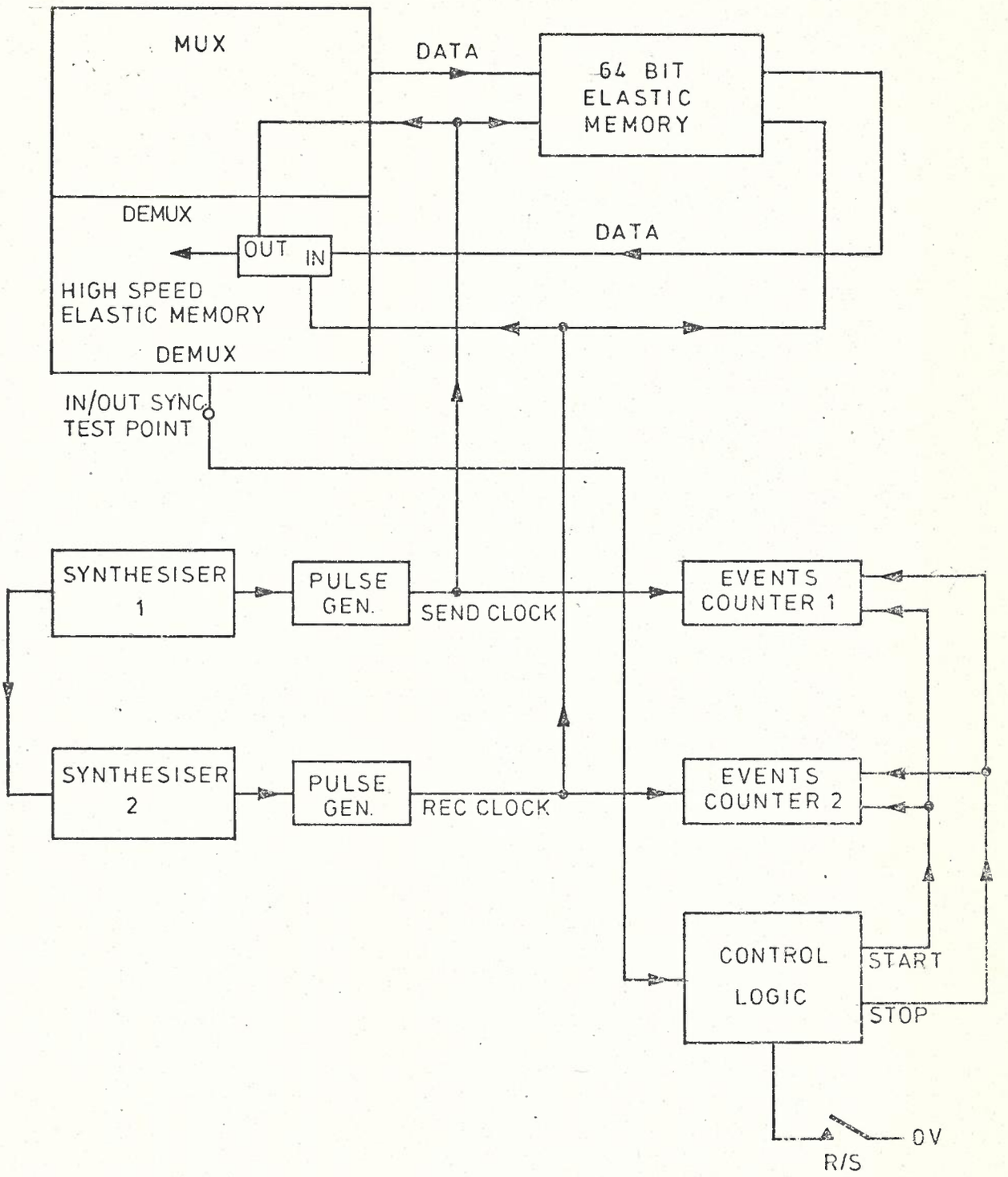


FIG. 6 TEST SETUP FOR MEASUREMENT OF DEMULTIPLEXER ELASTIC MEMORY CAPACITY

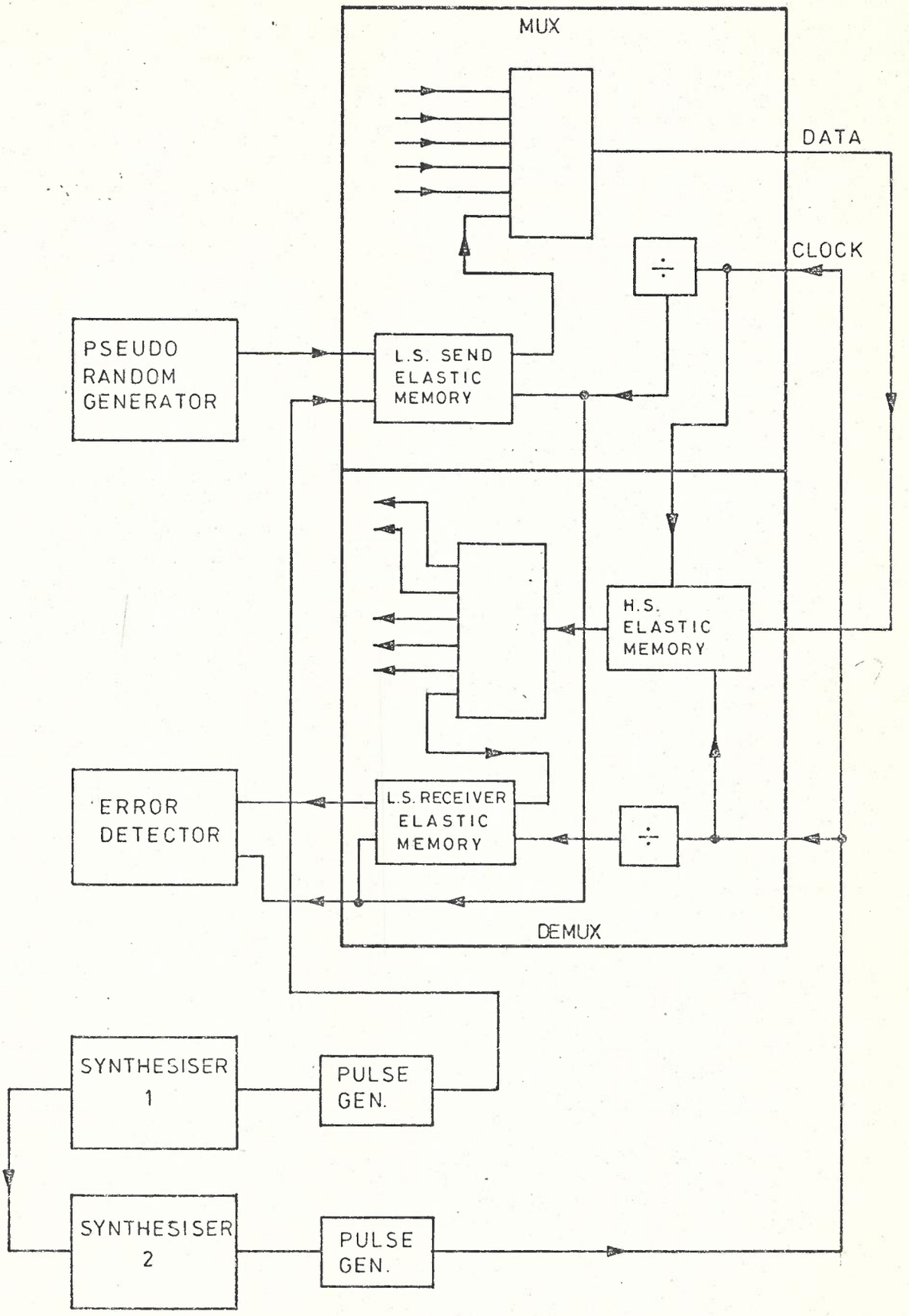


FIG. 7 TEST SETUP FOR MEASUREMENT OF LOW SPEED SEND ELASTIC MEMORY CAPACITY.

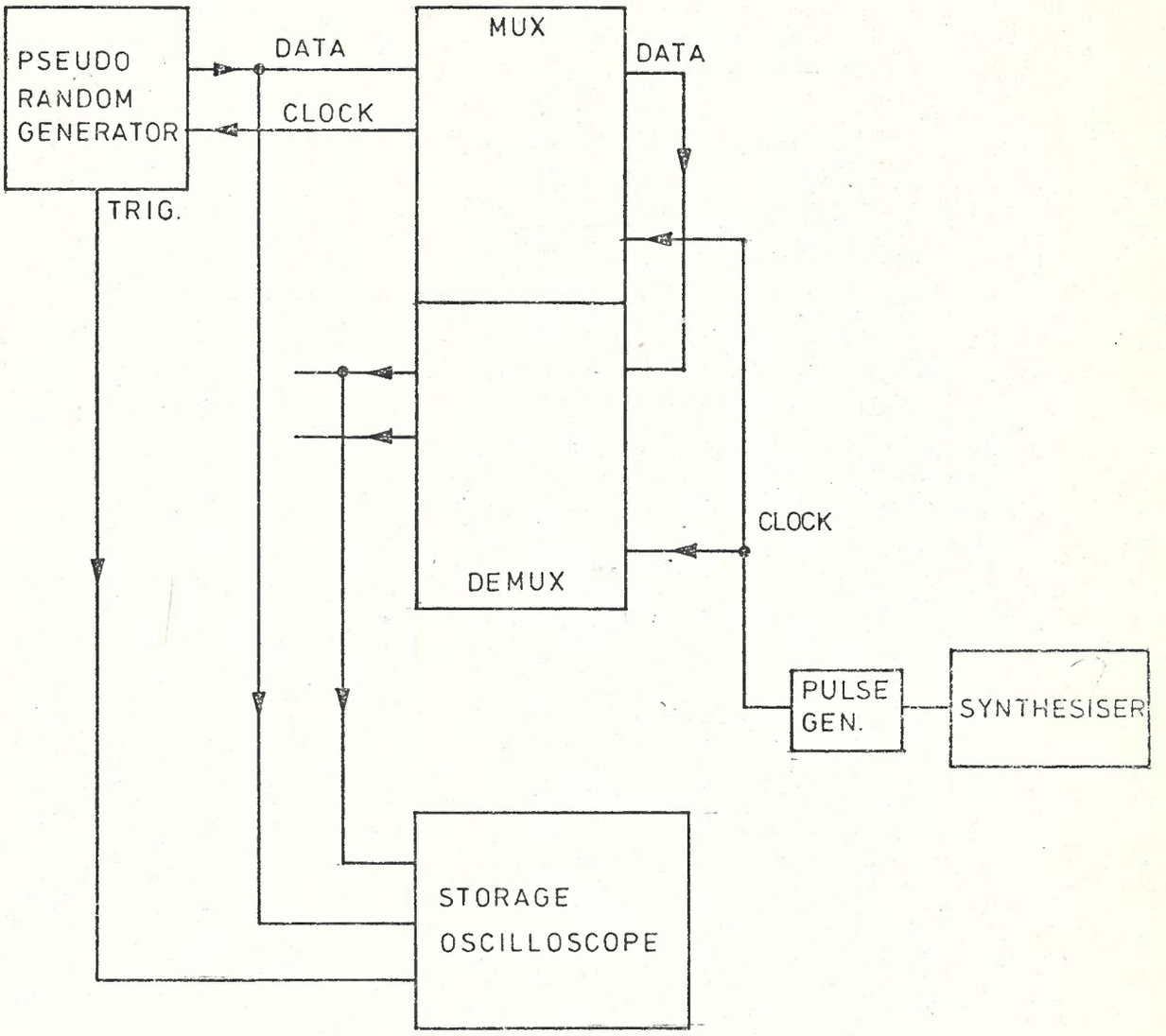


FIG. 8 TEST SETUP FOR MEASUREMENT OF CHANNEL DELAY.