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Research Laboratories Report 7253

Instrumentation Associated with Measurements on an Experimental Synchronous Digital Data Network

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Telecom Australia

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REPORT 7253

INSTRUMENTATION ASSOCIATED WITH MEASUREMENTS ON AN EXPERIMENTAL SYNCHRONOUS DIGITAL DATA NETWORK

BY R.B. COXHILL

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for Director, Research.

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Research Laboratories.

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(Its Report No. 7253

I. Coxhill, R.B.
1.DATA TRANSMISSION
2.INSTRUMENTATION
3.FREQUENCY DIVISION MULTIPLEXING
4.DATA MODEMS

SUMMARY

Telecom Australia plans to introduce in 1980 a new data communications network known as a Digital Data Network (DDN). In the early stages of the planned DDN, long haul transmission using data modems operating over a standard FDM group band circuit will be used.

Little is known of the characteristics of data transmission over group band circuits, and as a consequence, how these will affect operation of the proposed DDN. To investigate some of these aspects, the Research Laboratories of Telecom Australia has established a model synchronous data network. Instrumentation has been devised to automatically measure and record the key data transmission parameters associated with the model network.

This report gives a brief overview of the model network, and briefly describes the measurements performed on the network. Detailed circuits diagrams of the instrumentation used for controlling, measuring, and recording the measurements are included in the report, but descriptions of circuit operation are not given. Results of measurements are not included in this report.

CONTENTS

		Page
1.	INTRODUCTION	1
2.	MODEL NETWORK CONFIGURATION	1
3.	MEASUREMENT SETUP	2
4.	MEASUREMENT PERFORMED	2
	4.1 Bit Errors	2
	4.2 Error Seconds	2
	4.3 Breaks	2
	4.4 Slips	2
5.	FINAL REMARKS	2
6.	ACKNOWLEDGEMENT	3
7.	REFERENCES	3

Fig. 1 Actual Network Configuration
Fig. 2 Equivalent Network Configuration
Fig. 3 Functional Block Diagram

Circuit Diagrams

1. Line Break Interval Counter
2. Pseudo Random Generators
3. Multiplex & Control (1)
4. Multiplex & Control (2)
5. Phase Comparator, Buffer & Error Detector
6. Address Generator
7. Multiplex 2/3
8. Digital Clock
9. Punch Sequence Generator
10. Error Distribution Counter
11. Event Pulse Generator

RESEARCH LABORATORIES - REPORT 7253

INSTRUMENTATION ASSOCIATED WITH MEASUREMENTS ON AN EXPERIMENTAL SYNCHRONOUS DIGITAL DATA NETWORK

1. INTRODUCTION

Telecom Australia plans to introduce in 1980 a new data communications network known as a Digital Data Network (DDN). The network will initially be designed to support leased line data services. Long haul data transmission between network centres will be over the existing FDM network, at rates of 64 kbit/s, 72 kbit/s or multiples thereof. The 64 kbit/s data stream will be the basic building block of the DDN. For long haul transmission at 64 kbit/s, data modems operating over a standard group circuit will be used.

Little is known of the characteristics of data transmission over group band circuits, and as a consequence, how these will affect operation of the proposed DDN. To investigate some of these aspects, the Research Department has established a model synchronous data network. Instrumentation has been devised to automatically measure and record the key parameters associated with the model network.

This report gives a brief overview of the model network and the instrumentation used for controlling, measuring and recording all the aperiodical parameters (errors, breaks, slips). Detailed circuit diagrams are included in the report, but no description is given of circuit operation. A block diagram of the measurement setup is given, and this can be related to the circuit diagrams if necessary.

The periodical parameters of the model network (clock phase characteristics), are measured, analysed and recorded via microprocessor controlled instrumentation. Descriptions of the hardware and software associated with the microprocessor are the subject of a separate Research Laboratories Report (Ref. 1).

This report does not contain results of any measurements described in this report. However, some results of measurements are analysed in Ref. 2.

2. MODEL NETWORK CONFIGURATION

The model network has been configured as a three node master-slave network. Long haul group band circuits have been provided to various capital cities and are looped back at the distant location to enable testing of all circuits at one central location. Only one way transmission has been provided between nodes. Network configuration is shown in Figs. 1 and 2. Where possible, each interstate link consisted of a single transmission medium (either radio or co-axial cable) to enable better characterization of the network.

The model network was initially designed to operate at 48 kbit/s using N.E.C. data modems and associated V.S.B. equipment. The majority of testing was performed at this speed. Subsequently the hardware was modified to allow operation at 72 kbit/s, using data modems compatible with CCITT Recommendation V.36.

3. MEASUREMENT SETUP

A master clock at node 1 provides the source of timing for the model network. A slave clock (hereafter called nodal clock) at each of nodes 2 and 3 is synchronised to the master clock via timing derived from the receive modem at those nodes. At node 3 timing is derived from the modem receiver incoming from node 1. Should the incoming signal to a node fail, the nodal clocks will maintain accurate timing information.

At node 1, two pseudo random sequence generators driven by the master clock, provide test sequences that are each sent to nodes 2 and 3. At node 2, the synchronised nodal clock drives a third pseudo random sequence generator providing a test sequence that is sent to node 3. At node 3, incoming from node 2, a ± 4 bit elastic memory is included to allow for any phase differences between the paths from nodes 1 to 3, and from 1 to 3 via 2.

4. MEASUREMENTS PERFORMED

4.1 Bit Errors

The number of bit errors (maximum 998) for each 20 second period for each node was measured and recorded.

4.2 Error Seconds

The number of error-seconds occurring within the same 20 second period as above for each node was measured and recorded.

4.3 Breaks

The start time, finish time, and duration of any interruptions or "breaks" in the received signal for each node was measured and recorded. In the tests using 48 kbit/s modems, the scrambler and descrambler in the modems were bypassed to assist in detection of very short breaks. These were detected by monitoring the line signal received by the modem, and looking for periods of nine or more consecutive zeros. (As the transmitter uses a 511 bit pseudo random sequence, no more than 8 consecutive zeros should normally occur. In the tests using 72 kbit/s modems, the modem supplied, carrier fail detector was used for break detection.

In all tests a buffer was used to temporarily store up to 64 characters of break information, thus allowing recording of bursts of short breaks.

4.4 Slips

The time of occurrence of each elastic memory slip, together with under or overflow information, was measured and recorded.

All the above measurements were performed in real time. Results of measurements were punched onto paper tape together with periodic time of day information. The paper tapes were subsequently fed into the TACONET computer for detailed analysis.

5. FINAL REMARKS

Instrumentation devised to automatically measure and record the key parameters associated with a model DDN has been briefly described in this report. Over one year of virtually continuous recording has been achieved.

Some results of measurements have been analysed, and these are described in Ref. 2. At the time of writing this report, the measurement program has been suspended.

Experience gained in some areas of this project has assisted in the development of a fully automated, microprocessor controlled data test, which will be the subject of a future report.

6. ACKNOWLEDGEMENT

The author wishes to thank Mr J.A. Bylstra, who initiated the measurement program and designed most of the hardware and who also assisted the author in some design and development, Mr A.I. Domjan, for assistance and guidance during the measurement program, Mr P.J. Welby, who developed the computer analysis programs and provided guidance during the measurement program, Mr K.C. English who also developed computer analysis programs and Mr R. Webster, Mr J. Gillies, Mr G. Pridgeon, for their assistance in design and development of hardware.

7. REFERENCES

1. Webster, R., "Microprocessor Control of Clock Phase Measurements on an Experimental Synchronous Digital Data Network", Telecom Australia Research Laboratories, Report No. 7254, to be published.

2. Domjan, A.I., Duc, N.Q., Smith, B.M., "Loop Error Performance of some 48 kbit/s Groupband Data Circuits", Telecom Australia Research Laboratories, Transmission Systems Branch, Paper No. 9. November 1978.

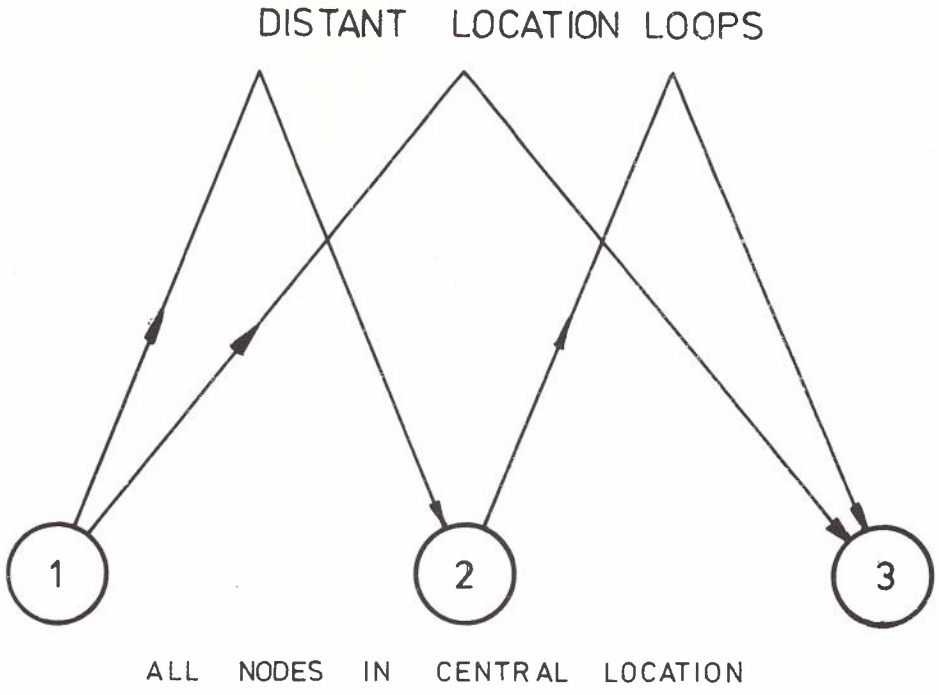

FIG.1. ACTUAL NETWORK CONFIGURATION

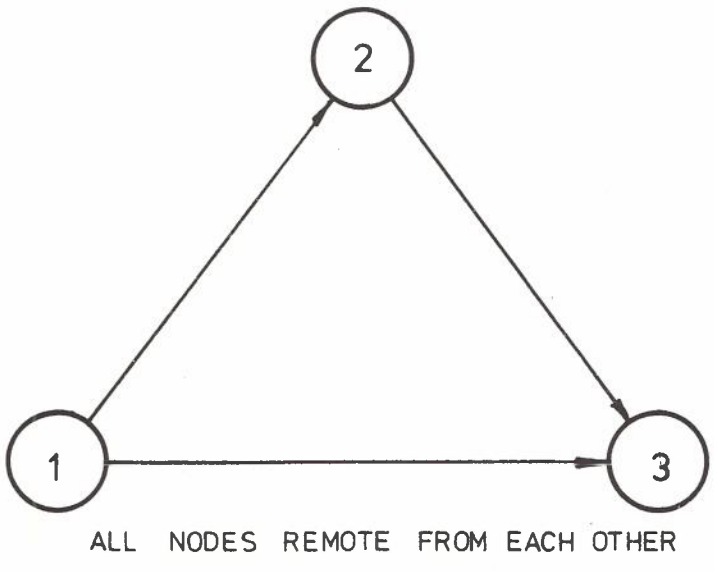

FIG. 2. EQUIVALENT NETWORK CONFIGURATION

RLR N°. 7253

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2				

INSTRUMENTATION FOR 48kBITS/sec DATA NETWORK MEASUREMENTS

FUNCTIONAL BLOCK DIAGRAM

CRSK-1334

SHEET 1 OF 1

CLOCK GENERATOR

LOAD AND CLOCK GENERATOR FOR BREAK COUNTER STORE

SHEET 2

PHASE COMPARATOR BUFFER & ERROR DETECTOR CRSK-1339

MODEM

BREAK DETECTOR

CLOCK GENERATOR FOR DECADE COUNTER

END OF BREAK RESET

START OF BREAK RESET

BREAK INDICATION CONTROL

BUFFER INPUT CONTROL

BUFFER OUTPUT CONTROL

CRSK-1568

POWER SUPPLY

TO ALL POINTS MARKED THUS

RPC-2442E

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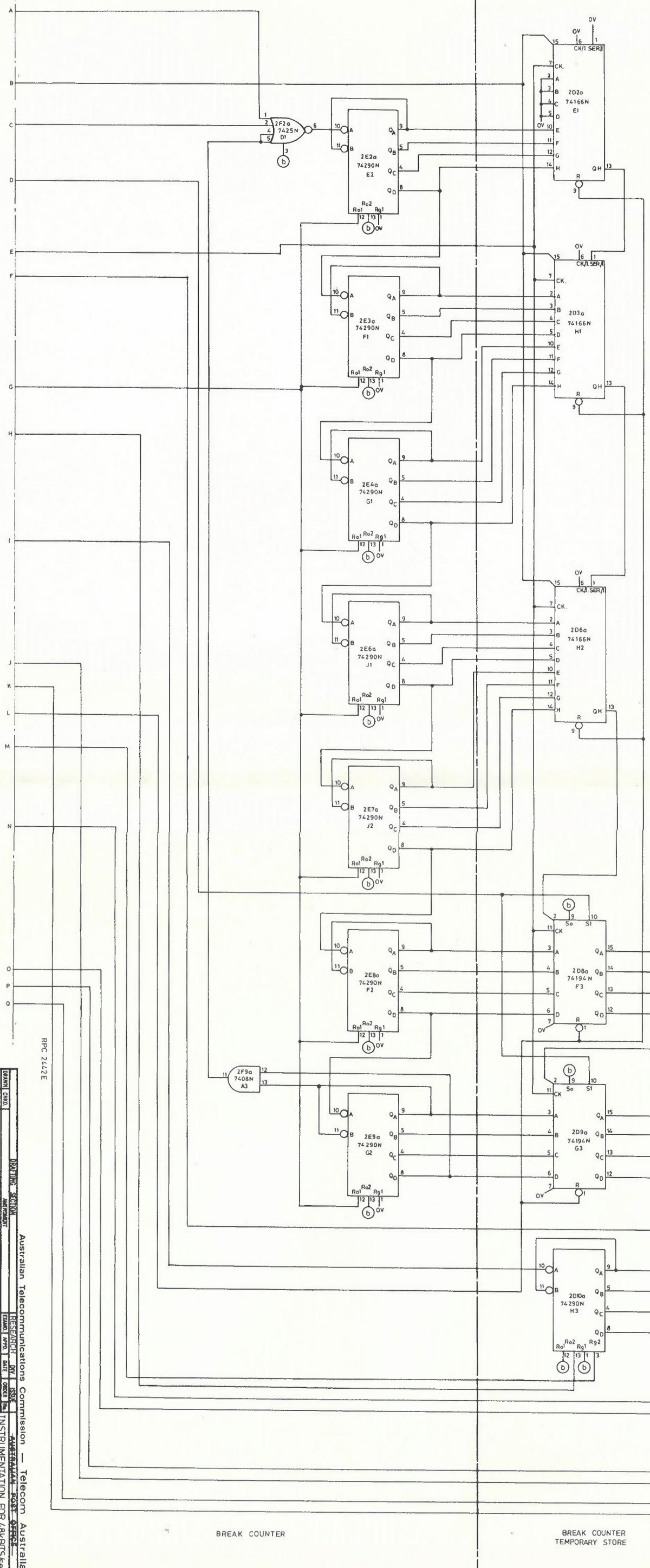
INSTRUMENTATION FOR 48 kBITS/sec DATA NETWORK MEASUREMENTS
LINE BREAK INTERVAL COUNTER
CIRCUIT DIAGRAM

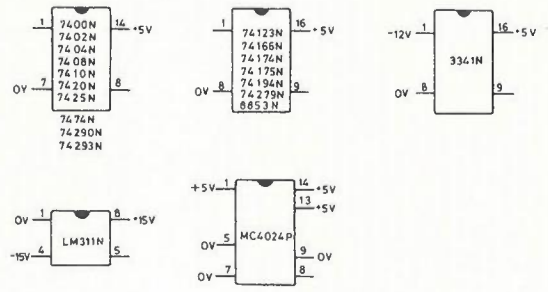
CRSK-1335 SHT. 1 OF 3

SHEET 1

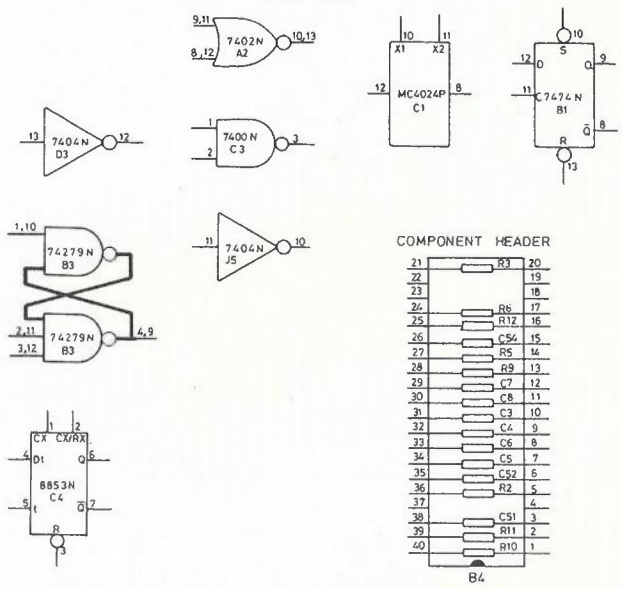


RPC 2442E

COMPONENT FACE



SPARE LOGIC



COMPONENT HEADER

(NOTE 1)
MULTIPLEX & CONTROL (1) CRSK-1337

ANGLE PROJECTION

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INSTRUMENTATION FOR 48kBITS/sec DATA NETWORK MEASUREMENTS
LINE BREAK INTERVAL COUNTER
CIRCUIT DIAGRAM
CRSK-1335
SHEET 2 OF 3

CRSK-1562
MASTER CLOCK
Bb31
Ab32
COMPONENT FACE
7400N 7402N 7404N 7420N 7451N 7474N 7486N 74164N 74293N
74279N
75110N
+5V
-5V
0V
PSEUDO RANDOM GENERATOR
ALL "0"S PROTECTION AND SYNC GENERATOR
SYNC 1
MONITOR POINT
Bb25
SINGLE ERROR INSERT
SWA
SINGLE ERROR INSERT 1,3
SWB
SINGLE ERROR INSERT 1,2
SWC
SINGLE ERROR INSERT 2,3
TTL TO V35 INTERFACE
SEND DATA OUT TO MODEM. LINK 1,3
SEND CLOCK OUT TO MODEM. LINK 1,3
SEND CLOCK OUT TO MODEM. LINK 1,2
SEND DATA OUT TO MODEM. LINK 2,3
SEND DATA OUT TO MODEM. LINK 1,2
SYNC 2
SYNC 3
Bb19
Bb13
Bb5
Bb4
Bb23
Bb1
Bb2
Bb17
Bb15
Ab19
Ab20
Ab5
B2
D5
F5
NODAL CLOCK
Ab21
SPARE LOGIC
TO ALL POINTS MARKED THUS
POWER SUPPLY
Ba32, Bb32
Aa1-32 Ba1-29
Ba30, Ba31
Bb26
+5V
0V
-5V

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INSTRUMENTATION FOR 48 kBITS/s DATA NETWORK MEASUREMENTS
PSUEDO RANDOM GENERATORS
CIRCUIT DIAGRAM
CRSK-1336
SHEET 1 OF DL

CRSK-1565

10 msec INTERRUPT. Ba22 / Ab15

CRSK-1338

Bb7 PH/SLIP(LINE)(1,2)* Ba18
Ab8 " " (NODAL)(2)* Bb20
Ab10 " " (LINE)(2,3)* Bb19
Ab9 " " (NODAL)(3)* Ba20
Ab11 " " (LINE)(1,3)* Ba19

1F8a 7415N J4 — 0V, S, A, B, C, D7, D6, D5, D4, D3, D2, D1, D0, Y

1C8b 74128N G2

1C9a 74128N G2

D11 [F5] 5082-2835 — R34 [F5] 82 — R35 [F5] 22 — F1-14 — I5-12

D24 [H2] 5082-2835 — R60 [H2] 82 — R61 [H2] 22 — F1-13 — I5-10

HEADER [I5] / HEADER [F1]

I5-5 F1-8
I5-3 F1-9
I5-1 F1-10
I5-7 F1-11

LINE DRIVERS

Ab3 Ab4 Ab5 Ba21

CONTROL CRSK-1338

Ab3 Ab4 Ab5 Ab6

CRSK-

CRSK-1561

Bb11 2^3 — 1F10c 7404N C3 — 1E10c 7437N D3 — Ab32
Bb12 2^4 — 1F11a 7404N C3 — 1E11a 7437N D3 — Ab31
Bb13 2^5 — 1F11b 7404N C3 — 1E11b 7437N D3 — Ab30
Bb14 2^6 — 1F12a 7404N C3 — 1E12a 7437N D3 — Ab24

SHEET 2 — 2^3 2^4 2^5 2^6

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J.M.F	P.H.		RAC	—	27-11-79	18742	4	MULTIPLEX AND CONTROL (1) CIRCUIT DIAGRAM

CRSK – 1337 — SHEET 1 OF 3

SHEET 1

CRSK-1339

Ab25	ERROR COUNT (1,2) 1		Aa24	
Ab24	" "	2	Ab25	1-1
Ab23	" "	3	Aa25	1-2
Ab22	" "	4	Ab26	1-3
Ab21	" "	5	Aa26	1-4
Ab20	" "	6	Ab27	1-5
Ab18	" "	7	Aa27	1-6
Ab17	" "	8	Ab28	1-7
Ab16	" "	9	Aa28	1-8
Ab15	" "	10	Ab29	1-9
Ab14	" "	11	Aa29	1-10
Ab13	" "	12	Aa30	1-11
				1-12
Ab25	ERROR COUNT (2,3) 1		Bb1	
Ab24	" "	2	Ba1	2-1
Ab23	" "	3	Bb2	2-2
Ab22	" "	4	Ba2	2-3
Ab21	" "	5	Bb3	2-4
Ab20	" "	6	Ba3	2-5
Ab18	" "	7	Bb4	2-6
Ab17	" "	8	Ba4	2-7
Ab16	" "	9	Bb5	2-8
Ab15	" "	10	Ba5	2-9
Ab14	" "	11	Bb6	2-10
Ab13	" "	12	Ba6	2-11
				2-12
Ab25	ERROR COUNT (1,3) 1		Ba9	
Ab24	" "	2	Bb10	3-1
Ab23	" "	3	Ba10	3-2
Ab22	" "	4	Bb11	3-3
Ab21	" "	5	Ba11	3-4
Ab20	" "	6	Bb12	3-5
Ab18	" "	7	Ba12	3-6
Ab17	" "	8	Bb13	3-7
Ab16	" "	9	Ba13	3-8
Ab15	" "	10	Bb14	3-9
Ab14	" "	11	Ba14	3-10
Ab13	" "	12	Bb15	3-11
				3-12

CRSK-1335
LINE BREAK INTERNAL COUNTER 1, 2 BOARD 1

Ab23	BREAK COUNT (1,2) 1		Ab23	
Ab22	" "	2	Ab22	6-1
Ab21	" "	3	Ab21	6-2
Ab20	" "	4	Ab20	6-3
Ab19	" "	5	Ab19	6-4
Ab18	" "	6	Ab18	6-5
Ab17	" "	7	Ab17	6-6
Ab16	" "	8	Ab16	6-7
Ab15	" "	9	Ab15	6-8
Ab14	" "	10	Ab14	6-9
Ab13	" "	11	Ab13	6-10
Ab12	" "	12	Ab12	6-11
				6-12

CRSK-1335
LINE BREAK INTERNAL COUNTER 2,3 BOARD 2

Ab23	BREAK COUNT (2,3) 1		Aa23	
Ab22	" "	2	Aa22	7-1
Ab21	" "	3	Aa21	7-2
Ab20	" "	4	Aa20	7-3
Ab19	" "	5	Aa19	7-4
Ab18	" "	6	Aa18	7-5
Ab17	" "	7	Aa17	7-6
Ab16	" "	8	Aa16	7-7
Ab15	" "	9	Aa14	7-8
Ab14	" "	10	Aa13	7-9
Ab13	" "	11	Aa12	7-10
Ab12	" "	12	Aa31	7-11
				7-12

CRSK-1335
LINE BREAK INTERNAL COUNTER 1,3 BOARD 3

Ab23	BREAK COUNT (1,3) 1		Ab11	
Ab22	" "	2	Ab10	8-1
Ab21	" "	3	Aa10	8-2
Ab20	" "	4	Ab9	8-3
Ab19	" "	5	Aa9	8-4
Ab18	" "	6	Ab8	8-5
Ab17	" "	7	Aa8	8-6
Ab16	" "	8	Ab7	8-7
Ab15	" "	9	Aa7	8-8
Ab14	" "	10	Ab6	8-9
Ab13	" "	11	Aa6	8-10
Ab12	" "	12	Aa15	8-11
				8-12

2^3 2^4 2^5 2^6

2E2a 74151N C5 — 2E4a 74151N B5 — 2E5a 74151N A5 — 2E6a 74151N D5 — 2E7a 74151N H5 — 2E8a 74151N G4

2C3a 74151N B4 — 2C4a 74151N A4 — 2C5a 74151N E4 — 2C7a 74151N E5 — 2C8a 74151N G5 — 2C9a 74151N J5

2B2a 74128N E1 — 2B3a 74128N F3 — 2B4a 74128N F3 — 2B4b 74128N F3 — 2B5a 74128N F3 — 2B5b 74128N E2 — 2B6a 74128N E2 — 2B7a 74128N E2 — 2B7b 74128N G1 — 2B8a 74128N G1 — 2B8b 74128N G1 — 2B9a 74128N G2

HEADER (F2)

D12	5082-2835	R36 82 [D2]	R37 22 [D2]	F2-19 — Ab10
D13	5082-2835	R38 82 [F5]	R39 22 [F5]	F2-1 — Ab9
D14	5082-2835	R40 82 [F5]	R41 22 [F5]	F2-2 — Ab8
D15	5082-2835	R42 82 [F5]	R43 22 [F5]	F2-3 — Ab7
D16	5082-2835	R44 82 [F5]	R45 22 [F5]	F2-4 — Ab14
D17	5082-2835	R46 82 [F5]	R47 22 [F5]	F2-5 — Ab13
D18	5082-2835	R48 82 [D2]	R49 22 [D2]	F2-20 — Ab5
D19	5082-2835	R50 82 [D2]	R51 22 [D2]	F2-21 — Ab4
D20	5082-2835	R52 82 [H2]	R53 22 [H2]	F2-7 — Ab3
D21	5082-2835	R54 82 [H2]	R55 22 [H2]	F2-8 — Ab2
D22	5082-2835	R56 82 [H2]	R57 22 [H2]	F2-9 — Ab1
D23	5082-2835	R58 82 [H2]	R59 22 [H2]	F2-10 — Ab12

POWER SUPPLY

-12V, +5V, Ba32, Bb32, 0V, Ba30, Ba31, Aa15, Ba15

C1 22, C2 0,1, C3 0,01, C12 0,01, C13 0,1, C30 0,1

R62 1k [F5] 40 — +5V — TO ALL POINTS MARKED THUS

COPONENT FACES

D2 (H2): (D24), R61, R60, (D23), R59, R58, (D22), R57, R56, D19, R51, R50, D18, R49, R48, D12, R37, R36, R31, D9, R32

F5: D17, R47, R46, D16, R45, R44, D15, R43, R42, D14, R41, R40, D13, R39, R38, R32, D10, R33, R34, D11, R35, R62

B1: R15, D1, R16, R17, D2, R18, R19, D3, R20, R21, D4, R22

B2: R23, D5, R24, R25, D6, R26, R27, D7, R28, R29, D8, R30

7404N 7408N 7437N 74128N 74290N — 3341 — 74151N 74153N

SPARE LOGIC

74128N E1 — 7404N B3

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M.S.	W.Y.	27-11-79	18742 3
D.P.	RAC		

INSTRUMENTATION FOR 48kBITS/s DATA NETWORK MEASUREMENTS

MULTIPLEX & CONTROL (1) CIRCUIT DIAGRAM

CRSK-1337 SHEET 2 OF 3

CRSK-1337

SPARE LOGIC

RESET ERROR COUNT 1,2

CRSK-1337 ERROR DET.

CRSK-1339 SLIP(S)

CRSK-1561

MUX & CONTROL CRSK-1337

BUFFER SLIP PULSE LENGTHENER

PHASE COMPARATOR SLIP LATCH

CRSK-1337

CRSK-1339 PHASE COMPARATOR SLIP

LINE NODAL

PL1,2

PN2

PL2,3

PN3

PL1,3

X-TAL 3072 kHz

C37 22 pF

48 kHz GENERATOR

CRSK-1339

JITTER CALIBRATE OUTPUT

CRSK-1562

÷104

PHASE DETECTOR

COMPARE COUNTER AND SWITCHES

COUNTER

S1-4

S5-8

S9-12

R12-15

R16-19

R20-23

SWITCH SETTINGS S9-12	S5-8	S1-4	PEAK TO PEAK JITTERS
6	2	4	100 %
3	1	2	50 %
1	5	6	25%

TO ALL POINTS MARKED THUS

POWER SUPPLY

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INSTRUMENTATION FOR 48 kBITS/s DATA NETWORK MEASUREMENTS

MULIPLEX & CONTROL 2 CIRCUIT DIAGRAM

CRSK-1338

SHEET 1 OF DL

ANGLE PROJECTION

LINE PHASE DET / CONTROL AND INDICATION

NODAL PHASE DET / CONTROL AND INDICATION

BUFFER CONTROL AND DISPLAY

NOTES:
1. IN A & C LINKS ONLY
2. ON A & C LINKS, CIRCUITRY MODIFIED AS FOLLOWS
   FROM F4, PIN4 (NORM. G2, PIN1) → 1G4b PIN 2; TO A4, PIN 1 (NORM. F3, PIN 15)
   FROM A5, PIN1 (NORM. A4, PIN4) → 1G4b PIN 3
3. IN B LINK ONLY
4. FOR OPERATION AT 72k BITS/SEC. CHANGE C5-C8 TO 2200.

ENCLOSED CIRCUIT ON B LINK ONLY.

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A.C.	P.H.		W.Y.	—	17-1-77	18707	1
M.S.	P.H.	MARGINAL INFORMATION	W.Y.	—	15-2-77	18722	2
I.C.R.	D.P.		R.A.C.	—	27-11-79	18742	3

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INSTRUMENTATION FOR 48kBITS/s DATA NETWORK MEASUREMENTS

PHASE COMPARATOR, BUFFER & ERROR DETECTOR CIRCUIT DIAGRAM

CRSK-1339 SHEET 1 OF 3

	1	2
SWA	INSERT JITTER CAL. SIGNAL(LINE)	RESET PHASE SLIP (LINE) INDICATOR
SWB	INSERT JITTER CAL. SIGNAL (NODAL)	RESET PHASE SLIP (NODAL) INDICATOR
SWC	RESET BUFFER SLIP INDICATOR	RESET BUFFER SLIP COUNT
SWD	MANUAL RESYNC	OUT OF SYNC INDICATOR RESET

PSEUDO RANDOM GENERATOR AND ERROR DETECTOR

ERROR COUNT UPDATE/RESET CONTROL

ALL "0"s PROTECTION AND SYNC GENERATOR

OUT OF SYNC DETECTOR

RESYNC CONTROL

998/999 SELECTOR

ERROR COUNTER

998 DETECTOR

OUTPUT LATCH

MULTIPLEX CONTROL 2 CRSK-1338

ERROR DISTRIBUTION COUNTER CRSK-1567

MULTIPLEX & CONTROL (1) CRSK-1337

MONITOR POINT TRIG OUT

ERROR DISTRIBUTION COUNTER CRSK-1567

COUNT ERROR (ER)

POWER SUPPLY

COMPONENT FACE

SPARE LOGIC

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INSTRUMENTATION FOR 48kBITS/s DATA NETWORK MEASUREMENTS

PHASE COMPARATOR BUFFER & ERROR DETECTOR CIRCUIT DIAGRAM

CRSK-1339 SHEET 2 OF 3

CRSK-

Bb29 CARRY HOURS I/P — Bb15

Ab1 EVENT CLOCK — Bb17

DIGITAL CLOCK

÷11 ÷21 ÷19 ÷2

7404N B1 7404N J4 7408N A5 7404N H3 7404N G4 7404N A1

74161N A2 74161N B2 74161N C2 74161N C3 74161N B3 74161N A3

74188AN D3 74188AN E3

+5V +5V +5V +5V +5V +5V +5V +5V

R1–R8 8x2k [F2]

SELECT ÷11, ÷21 / ÷19, ÷2

7474N H5 7474N H1 7400N D5 7400N H4 7400N G3

74174N J5 7474N D2

7400N C5 7474N C4

ENABLE TIME

CRSK-1568

Bb6 T+ SPACE — Bb11

CRSK-1337

CRSK-1566

CRSK-1563

Ab18 Ab16 Bb16

Ab17 Ab19 Bb12 Bb5 Bb17

Ab15 Ab15

Ab14 Ab16 Bb11 Bb17 Bb4 Ba16

Bb10 Bb16

Ab12 Bb18

Ab13 Bb3

Ab10 Bb19

Bb9 Ba7

Ab11 Bb2

Ab8 Bb20

Bb8 Bb7

Ab9 Bb1

RESET TIME

7400N H4 7425N E2 7404N J4

SPACE

STORE TIME AND RESET AT SPACE TIME SLOT

TIME

7420N F4 7402N D4

Ab7 Bb8

7430N J3

SELECT CR / LF

Ab2 Ab17

Ab1 Bb15

Ab3 Bb6

Bb13 Ba17

74128N A1 74128N C1

LINE DRIVERS

SHEET 2

A B C D E K L M N P Q

SHEET 2

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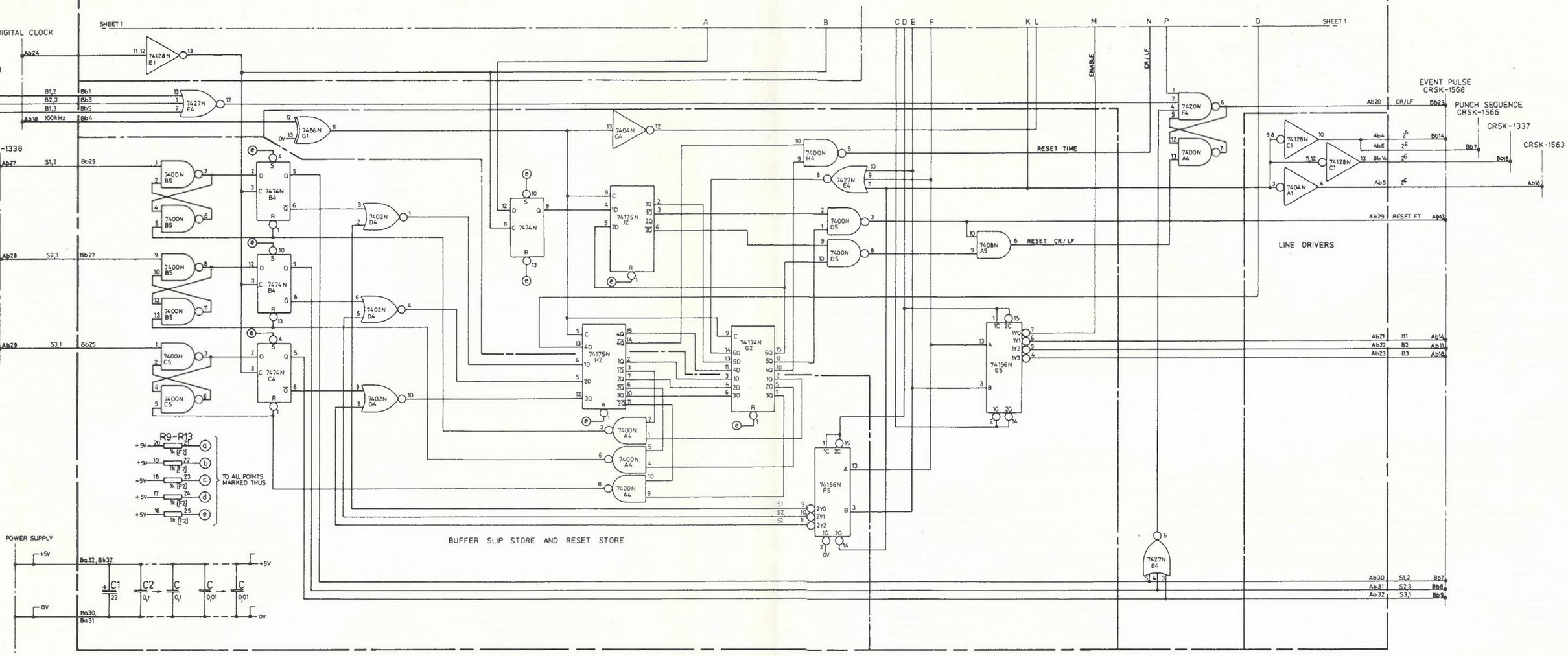
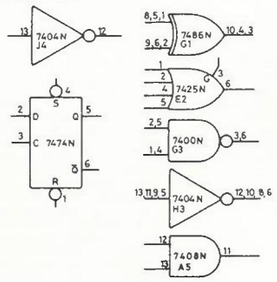
INSTRUMENTATION FOR 48kBIT/s DATA NETWORK MEASUREMENTS

ADDRESS GENERATOR CIRCUIT DIAGRAM

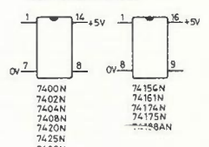
CRSK–1561 SHEET 1 OF 2



SPARE LOGIC



COMPONENT FACES



COMPONENT HEADER

PROM PROGRAMMING AT E3

ADDRESS					OUTPUTS								
E	D	C	B	A	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	FUNCTION
0	1	1	0	1	0	0	0	0	0	0	0	0	E1,2
0	1	1	1	0	0	0	0	0	1	0	0	0	E2,3
0	1	1	1	1	0	0	0	1	0	0	0	0	E1,3
1	0	0	0	0	0	0	1	0	0	0	0	0	TIME
1	0	0	0	1	1	1	1	1	1	0	0	0	SPACE
1	0	0	1	0	1	1	1	1	1	0	0	0	"
1	0	0	1	1	1	1	1	1	1	0	0	0	"
1	0	1	0	0	1	1	1	1	1	0	0	0	"
1	0	1	0	1	1	1	1	1	1	0	0	0	"
1	0	1	1	0	1	1	1	1	1	0	0	0	"
1	0	1	1	1	1	1	1	1	1	0	0	0	"
1	1	0	0	0	1	1	1	1	1	0	0	0	"
1	1	0	0	1	1	1	1	1	1	0	0	0	"
1	1	0	1	0	1	1	1	1	1	0	0	0	"
1	1	0	1	1	1	1	0	1	1	1	1	1	CR
1	1	1	0	0	1	1	0	1	1	1	1	0	LF
1	1	1	0	1	0	1	0	0	0	0	0	0	S1
1	1	1	1	0	0	1	0	0	1	0	0	0	S2
1	1	1	1	1	0	1	0	1	0	0	0	0	S3

PROM PROGRAMMING AT D3

ADDRESS					OUTPUTS								
E	D	C	B	A	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	FUNCTION
0	0	1	0	1	1	1	0	1	1	0	0	0	ST1
	0	1	1	0	0	0	1	0	1	0	0	0	B1
	0	1	1	1	1	1	0	1	1	0	0	1	FT1
	1	0	0	0	1	1	0	1	1	0	1	0	ST2
	1	0	0	1	0	0	1	1	0	0	0	0	B2
	1	0	1	0	1	1	0	1	1	0	1	1	FT2
	1	0	1	1	1	1	0	1	1	1	0	0	ST3
	1	1	0	0	0	0	1	1	1	0	0	0	B3
	1	1	0	1	1	1	0	1	1	1	0	1	FT3
	1	1	1	0	1	1	0	1	1	1	1	1	CR
	1	1	1	1	1	1	0	1	1	1	1	0	LF

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INSTRUMENTATION FOR 48kBIT/s DATA NETWORK MEASUREMENTS

ADDRESS GENERATOR

CIRCUIT DIAGRAM

CRSK– 1561

SHEET 2 OF 2

CRSK-1561

TIME DAYS / HOURS

TIME MINUTES / SECONDS

DIGITAL CLOCK CRSK-1565

HEADER IN POSITION F5

SHT. 2

SELECT DAYS / HOURS MINUTES / SECONDS

CRSK-1337 (HEADER IN POSITION F2)

ALL '0's DETECTOR

EVENT PULSE CRSK-1568

PUNCH SEQUENCE CRSK-1566

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INSTRUMENTATION FOR 48 kbit/s DATA NETWORK MEASUREMENTS
MULTIPLEX 2/3
CIRCUIT DIAGRAM

CRSK-1563 SHEET 1 OF 2

SHT. 1

POWER SUPPLY

+5V

0V

C1

C2

C

ERROR DISTRIBUTION COUNTER CRSK-1567

ERROR SECONDS COUNTER

CRSK-1339

Bb8 S1 2 POLARITY

Bb8 S2 3 POLARITY

Bb8 S1 3 POLARITY

SELECT DAYS / HOURS OR MINUTES / SECONDS

SELECT TIME OR ERROR SECONDS

SELECT SLIP POLARITY OR ERROR SECONDS

PUNCH SEQUENCE CRSK-1566

COMPONENT FACES

7400N
7402N
7404N
7408N
7410N
7425N
74128N

74151N
74157N
74153N

SPARE LOGIC

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INSTRUMENTATION FOR 48 kbit/s DATA NETWORK MEASUREMENTS

MULTIPLEX 2/3

CIRCUIT DIAGRAM

CRSK-1563

SHEET 2 OF 2

CRSK-1565

INSTRUMENTATION FOR 48 kBITS DATA NETWORK MEASUREMENTS DIGITAL CLOCK CIRCUIT DIAGRAM

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SHEET 1 OF 1

ANGLE PROJECTION

CRSK-1337 100Hz Ab15

CRSK-1568 EVENT CLOCK Ab1 Bb17 Ab19

CRSK-1561

80mS

+5V RESET SECONDS 4,7k KK28 KK27 KK26 OV

CRSK-1563

100kHz 10kHz 1kHz 100Hz 10Hz 1Hz

÷10^5

LSB Bb7 FS 39 Bb8 FS 38 Bb9 FS 37 Bb10 FS 36

CRSK-1337 20 sec PULSE Ab14 Ba23 SEC.

SECONDS COUNTER

MSB Bb6 FS 31 Bb5 FS 32 Bb4 FS 33 Bb3 FS 34

MANUAL CONTROL MINUTES KK23 KK24 KK25

MANUAL CONTROL OVERIDE KK1 KK2 KK3

LSB Bb12 FS 29 Bb13 FS 28 Bb14 FS 27 Bb15 FS 26

MINUTES COUNTER

MSB Bb19 FS 22 Bb18 FS 23 Bb17 FS 24 Bb16 FS 25

MIN.

MANUAL CONTROL HOURS KK5 KK6 KK4

X

LSB Bb24 FS 17 Bb23 FS 16 Bb22 FS 15 Bb21 FS 14

HOURS COUNTER

MSB Bb25 FS 10 Bb26 FS 11 Bb27 FS 12 Bb28 FS 13

HOURS

MANUAL CONTROL DAYS KK2A KK3A KK1A

LSB Ab7 FS 9 Ab8 FS 8 Ab9 FS 7 Ab10 FS 6

DAYS COUNTER

MSB Ab6 FS 2 Ab5 FS 3 Ab4 FS 4 Ab3 FS 5

DAYS

EVENT PULSE CRSK-1568

TO RUBIDIUM VAPOUR FREQUENCY STANDARD (MASTER CLOCK) 5MHz

C1 0,001 R3 3,9k R2 1,2k 24

÷5 ÷10

C2 22 C3 0,1 C13 0,1 C14 0,01 C31 0,01

Ba32, Bb32 Ba30, Ba31 Ba15 Aa15

Ab16 100kHz Ab30

PUNCH SEQUENCE

Ab17 100kHz Ab22 CRSK-1566

Ab18 100kHz Bb4 CRSK-1561

Ab13 1MHz Ab17

ERROR DIST. CONNECTOR CRSK-1567

EVENT PULSE Ab21 Ab32

TRANSFER PULSE Ab22 Ab15

CRSK-1561

TRANSFER PULSE Bb7 Ab24

CARRY HOURS Bb15

R1 1k [F5] TO ALL POINTS MARKED THUS

SPARE LOGIC

COMPONENT FACE

F5

PUNCH
PUNCH DATA
Ab 21
7404N J2
74175N G2
7400N J1
74123N F2
125µs
74128N E4
74161N F5
74155N F4
7402N E3
7425N E2
7404N J2
CRSK-1565
Ab17
100kHz
Ab22
74128N E4
PUNCH READY
Ab23
7404N J2
74175N G3
7400N G1
74175N G4
7402N F3
74175N G5
+5V
R1 F1
C42 20k 0033
R2 82
R3 22
V1 5082-2385
PUNCH
Ab24
PI
7400N D2
7404N D3
CRSK-1568
RMS ADDRESS CLOCK
Bb10
Bb22
+5V
R4 F1
C43 10k 00056
16µs
74123N F2
74175N G5
CRSK-1563
Bb17 2^2
Ab20
Bb18 2^3
Ab19
LSB
CK/IN SER SHIFT I/P LOAD
74166N H3
74161N E1
74155N D1
Bb19 2^1
Ab18
Bb20 2^0
Ab17
Bb13 2^3
Ab16
Bb14 2^2
Ab15
Bb15 2^1
Ab14
Bb16 2^0
Ab13
Bb9 2^3
Ab12
Bb10 2^2
Ab11
Bb11 2^1
Ab10
Bb12 2^0
Ab9
Bb5 2^3
Ab8
Bb6 2^2
Ab7
7404N J3
74198N H2
S/L S/R S1 S0
Bb7 2^1
Ab6
Bb8 2^0
Ab5
Bb1 2^3
Ab4
Bb2 2^2
Ab3
Bb3 2^1
Ab2
Bb4 2^0
Ab1
7404N J5
MSB
74198N H5
STR SEL
74157N C4
74157N C3
CRSK-1561
Ab9 2^0
Bb1
Ab11 2^1
Bb2
Ab13 2^2
Bb3
Ab16 2^3
Bb4
Ab19 2^4
Bb5
Ab3 2^5
Bb6
Ab6 2^6
Bb7
Ab7 2^7
Bb8
74188N B5
74188N C5
74188N D5
74188N E5
74188N A5
7404N B3
7402N A4
R21-28 8X2.2k
R29-32 4X2.2k
R33-35 3X2.2k
TO ALL POINTS MARKED THUS
V2 8X5082-2385
R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20
82
22
Bb14 D3
Bb13 D2
Bb12 D1
Bb11 D0
Bb18 D7
Bb17 D6
Bb16 D5
Bb15 D4
B2
POWER SUPPLY
C41 C3 C2 C1
0,1
22
Ba32 Bb32
Aa1-32 Ba1-31
COMPONENT FACES
7400N 7402N 7404N 74128N
74123N 74151N 74155N 74157N 74161N 74166N 74175N 74188N 8X50B2-2385
74198N
D4
F1
B2

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INSTRUMENTATION FOR 48kBITS DATA NETWORK MEASUREMENTS

PUNCH SEQUENCE GENERATOR CIRCUIT DIAGRAM

CRSK-1566

SHEET 1 OF 1

CRSK-1562 MASTER CLOCK — Ab31 72 kHz. — Bb25

CRSK-1565 Ab33 DIGITAL CLOCK — 1MHz. — Bb21

ERROR PAUSE CRSK-1339

Bb15 RESET LINK A — Ab22

Ab5 LINK A — Ab21

Ab5 LINK B — Ab19

Ab5 LINK C — Ab17

Bb15 RESET LINK C — Ab18

Bb15 RESET LINK B — Ab20

ADDRESS GENERATOR CRSK-1561 — 2^3, 2^4

S1 — 200msec, 250msec, 500msec, 1sec

R5-8 4X1,2k

Bb11 Bb13 — CRSK-1339 ERROR DETECTOR

MULTIPLEX 2/3 CRSK-1563 — Bb28 Bb27 Bb26 Bb25 Ab32 Ab31 Ab30 Ab29

ERROR SECONDS COUNT

POWER SUPPLY — +5V, 0V — Bc32, Bc31, Bc30, Ac1-32, Bc1-29 — C1 0,1; C27 0,1; C28 0,01; C41 0,01

COMPONENT FACE

E1 — R1 1,2k; R2 1,2k; R3 1,2k; R4 1,2k; R7 1,2k; R8 1,2k; R6 1,2k; R5 1,2k

R1 R2 R3 R4 [E1] — 4X1,2k — TO ALL POINTS MARKED THUS

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INSTRUMENTATION FOR 48kBIT/s DATA NETWORK MEASUREMENTS

ERROR DISTRIBUTION COUNTER

CIRCUIT DIAGRAM

CRSK-1567 — SHEET 1 OF 1

STORE AND BREAK COUNT
UPDATE CONTROL FOR B1/2

COMPONENT FACE

TO ALL POINTS MARKED THUS

STORE AND BREAK COUNT
UPDATE CONTROL FOR B2/3

STORE AND BREAK COUNT
UPDATE CONTROL FOR B1/3

POWER SUPPLY

CR/LF CONTROL

PUNCH CONTROL

CRSK-1561
ADDRESS GENERATOR

CRSK-1565
DIGITAL CLOCK

DIGITAL CLOCK
CRSK-1565
EVENT PULSE

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CRSK-1568

INSTRUMENTATION FOR 48KBITS/s DATA NETWORK MEASUREMENTS

EVENT PULSE GENERATOR CIRCUIT DIAGRAM

SHEET 1 OF 1